February 2007

National Semiconductor

LMX9820A
Bluetooth® Serial Port Module

1.0 General Description

The National Semiconductor LMX9820A Bluetooth Serial Port module is a highly integrated radio, baseband controller, and memory device implemented on an FR4 substrate. All hardware and firmware is included to provide a complete solution from antenna from the complete lower and upper layers of the Bluetooth stack, up to the application support layers including the Generic Access Profile (GAP), the Service Discovery Application Profile (SDAP), and the Serial Port Profile (SPP). The module includes a configurable service database to fulfill service requests for additional profiles on the host. The LMX9820A features a small form factor (10.1 x 14.1 x 2.0 mm) design, which solves many of the challenges associated with compact system integration. Moreover, the LMX9820A is pre-qualified as a Bluetooth Integrated Component. Conformance testing through the Bluetooth qualification program enables a fast time to market after system integration by ensuring a high degree of compliance and interoperability.

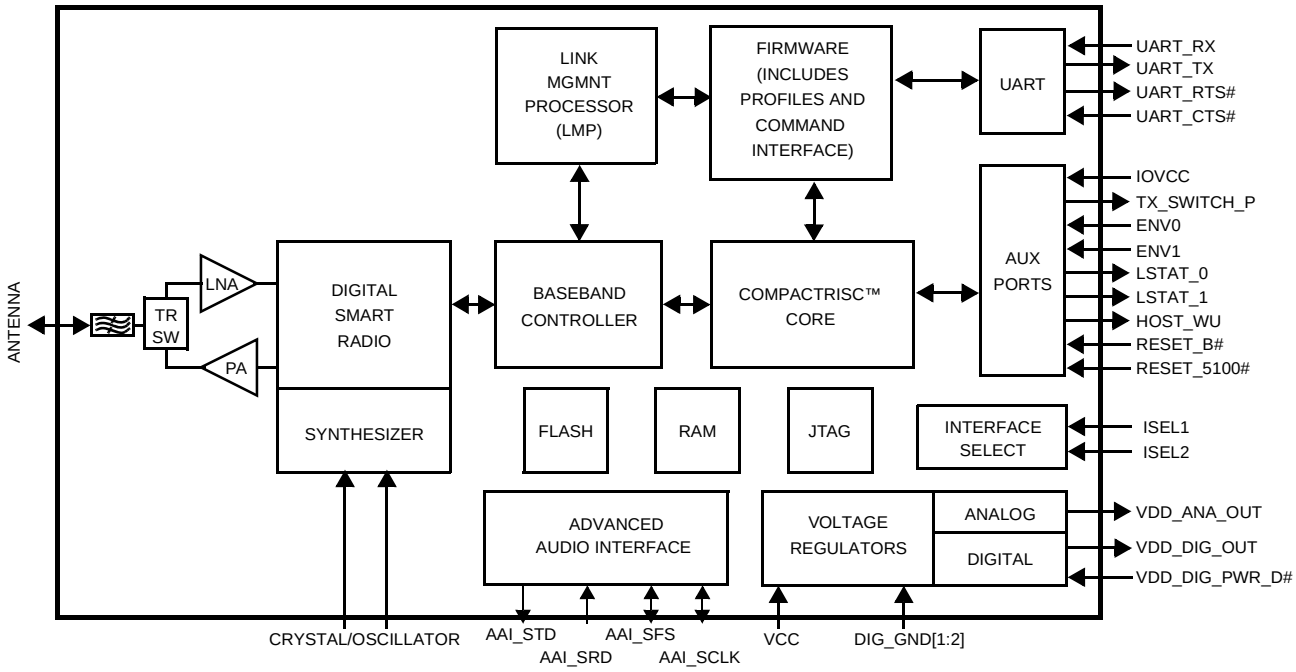
Based on National's CompactRISC™ 16-bit processor architecture and Digital Smart Radio technology, the LMX9820A is optimized to handle the data and link management processing requirements of a Bluetooth node.

The firmware supplied with this device offers a complete Bluetooth (v1.1) stack including profiles and command interface. This firmware features point-to-point and point-to-multipoint link management supporting data rates up to the theoretical maximum over RFComm of 704 kbps. The internal memory supports up to three active Bluetooth data links and one active SCO link.

1.1 APPLICATIONS

- Personal Digital Assistants
- POS Terminals
- Data Logging Systems
- Audio Gateway applications

2.0 Functional Block Diagram



3.0 Features

- Bluetooth version 1.1 qualified
- Implemented in CMOS technology on FR4 substrate
- Temperature Range: -40°C to +85°C
- FCC certified on LMX9820ADONGLE, FCC ID ED9LMX9820ASM

3.1 DIGITAL HARDWARE

- Baseband and Link Management processors
- CompactRISC Core
- Integrated Memory:
  - Flash
  - RAM
- UART Command/Data Port:
  - Support for up to 921.6k baud rate
- Auxiliary Host Interface Ports:
  - Link Status
  - Transceiver Status (Tx or Rx)
  - Operating Environment Control:
    - Default Bluetooth mode
    - In System Programming (ISP) mode
- Advanced Power Management (APM) features
- Advanced Audio Interface for external PCM codec

3.2 FIRMWARE

- Complete Bluetooth Stack including:
  - Baseband and Link Manager
  - L2CAP, RFCOMM, SDP
  - Profiles:
    - GAP
    - SDAP
    - SPP
- Additional Profile support on host for any SPP based profile, like
  - Dial Up Networking (DUN)
  - Facsimile Profile (FAX)
  - File Transfer Protocol (FTP)
  - Object Push Profile (OPP)
  - Headset (HSP)
  - Handsfree Profile (HFP)
- On-chip application support including:
  - Command Interface:
    - Link setup and configuration (also Multipoint)
    - Configuration of the module
    - In-System Programming (ISP)
    - Service database modifications
    - Default connections
  - UART Transparent mode
  - Different Operation modes:
    - Automatic mode
    - Command mode

3.3 DIGITAL SMART RADIO

- Accepts external clock or crystal input:
  - 12 MHz
  - 20 ppm cumulative clock error required for Bluetooth
  - Secondary 32.768kHz oscillator for low-power modes.
- Synthesizer:
  - Integrated VCO and loop filter
  - Provides all clocking for radio and baseband functions
- Antenna Port (50 ohms nominal impedance):
  - Embedded front-end filter for enhanced out of band performance
- Integrated transmit/receive switch (full-duplex operation via antenna port)
- Typical -81 dBm input sensitivity
- 0 dBm typical output power

3.4 PHYSICAL DIMENSIONS

- Compact size: 10.1mm x 14.1mm x 2.0mm
- Complete system interface provided in Land Grid Array on underside for surface-mount assembly

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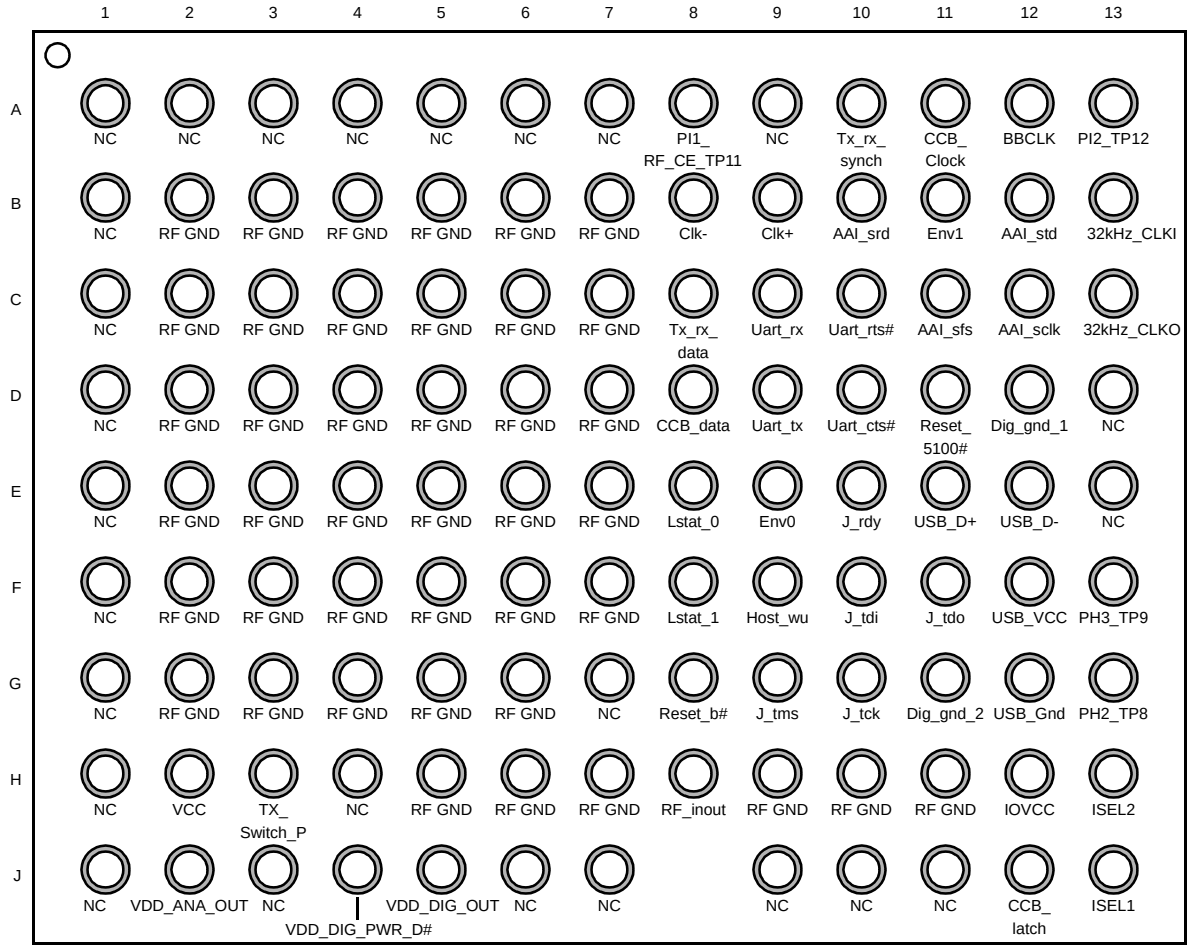
4.0 Connection Diagram



X-Ray (Top View)

Figure 1. Connection Diagram

Table 1. Ordering Information

Order Number	Spec	Shipment Method
LMX9820ASM		Tape & Reel 153 pcs
LMX9820ASMX		Tape & Reel 1000 pcs
LMX9820ASM	NOPB	Tape & Reel 153 pcs
LMX9820ASMX	NOPB	Tape & Reel 1000 pcs

5.0 Pad Descriptions

Table 2. System Interface Signals

Pad Name	Pad Location	Direction	Description
Clk-	B8	Input	**Xtal g or Negative Clock Input.** Typically connected along with XTAL_D to an external surface-mount AT-cut crystal. Leave not connected in case Clk+ is connected to external crystal oscillator.
Clk+	B9	Input	**Xtal d or Positive Clock Input.** Typically connected along with XTAL_G to an external surface-mount AT-cut crystal. Can also be configured as a frequency input when using an external crystal oscillator. When configured as a frequency input, typically connected to an external Temperature Compensated Crystal Oscillator (TCXO) through an Alternating Current (AC) coupling capacitor.
32kHz_CLKI	B13	Input	**32 kHz Clock input.** If not used connect to ground.
32kHz_CLKO	C13	Output	**32 kHz Clock Output.** If not used then treat as no connect.
RF_inout	H8	Input/Output	**RF Antenna Port.** 50Ω nominal impedance. Typically connected to an antenna through a 6.8 pF capacitor.
ISEL2	H13	Input	**Module Interface Select Input Bit 1**
ISEL1	J13	Input	**Module Interface Select Input Bit 0**

Table 3. USB Interface Signals (not supported by LMX9820A firmware)

Pad Name	Pad Location	Direction	Description
USB_V_{CC}	F12	Input	**USB Transceiver Power Supply +** [1]
USB_D+	E11	Input/Output	**USB Data Positive** [1]
USB_D-	E12	Input/Output	**USB Data Negative** [1]
USB_Gnd	G12	Input	**USB Transceiver Ground**. Connect to GND.

1. Treat as no connect. Pad required for mechanical stability.

Table 4. UART Interface Signals

Pad Name	Pad Location	Direction	Description
Uart_tx	D9	Output	**UART Host Control Interface Transport, Transmit Data**
Uart_rx	C9	Input	**UART Host Control Interface Transport, Receive Data**
Uart_rts#	C10	Output	**UART Host Control Interface Transport, Request to Send** [1]
Uart_cts#	D10	Input	**UART Host Control Interface Transport, Clear to Send** [2]

1. Treat as no connect if not used. Pad required for mechanical stability.
2. Connect GND if not used.

Table 5. Auxiliary Ports Interface Signals

Pad Name	Pad Location	Direction	Description
IOV_{CC}	H12	Input	**2.85V to 3.6V Logic Threshold Program Input.**

5.0 Pad Descriptions (Continued)

Table 5. Auxiliary Ports Interface Signals (Continued)

Pad Name	Pad Location	Direction	Description
Reset_b#	G8	Input	**Reset for Smart Radio.** Connect to Reset_5100.
Reset_5100#	D11	Input	**Reset for Baseband processor.** Low active, either connect to host or use pull-up with max. 1KΩ resistor.
Lstat_0	E8	Output	**Link Status Bit 0**
Lstat_1	F8	Output	**Link Status Bit 1**
Host_wu	F9	Output	**Host Wakeup**
Env0	E9	Input	**Module Operating Environment Bit 0**
Env1	B11	Input	**Module Operating Environment Bit 1**
TX_Switch_P	H3	Output	**Transceiver Status.** 0 = Receive; 1 = Transmit.

Table 6. Audio Port Interface Signals

Pad Name	Pad Location	Direction	Description
AAI_srd	B10	Input	**Advanced Audio Interface Receive Data Input** [1]
AAI_std	B12	Output	**Advanced Audio Interface Transmit Data Output** [1]
AAI_sfs	C11	Input/Output	**Advanced Audio Interface Frame Synchronization** [1]
AAI_sclk	C12	Input/Output	**Advanced Audio Interface Clock** [1]

1. Treat as no connect if not used. Pad required for mechanical stability.

Table 7. Test Interface Signals

Pad Name	Pad Location	Direction	Description
J_rdy	E10	Output	**JTAG Ready** [1]
J_tdi	F10	Input	**JTAG Test Data** [1]
J_tdo	F11	Input/Output	**JTAG Test Data** [1]
J_tms	G9	Input/Output	**JTAG Test Mode Select** [1]
J_tck	G10	Input	**JTAG Test Clock** [1]
PI1_RFCE_TP11	A8	Test Pin	**Module Test Point** [1]
PI2_TP12	A13	Test Pin	**Module Test Point** [1]
Tx_rx_data	C8	Test Pin	**Module Test Point** [1]
Tx_rx_synch	A10	Test Pin	**Module Test Point** [1]
CCB_Clock	A11	Test Pin	**Module Test Point** [1]
CCB_data	D8	Test Pin	**Module Test Point** [1]
CCB_latch	J12	Test Pin	**Module Test Point** [1]
BBCLK	A12	Test Pin	**Module Test Point** [1]
PH3_TP9	F13	Test Pin	**Module Test Point** [1]
PH2_TP8	G13	Test Pin	**Module Test Point** [1]

1. Treat as no connect. Pad required for mechanical stability.

5.0 Pad Descriptions (Continued)

Table 8. Power, Ground, and No Connect Signals

Pad Name	Pad Location	Direction	Description
NC	A1, A2, A3, A4, A5, A6, A7, A9, B1, C1, D1, D13, E1, E13, F1, G1, G7, H1, J1, J3, J6, J7, J9, J10, J11	No Connect	**No Connect.** Pad required for mechanical stability.
RF GND [1]	B2, B3, B4, B5, B6, B7, C2, C3, C4, C5, C6, C7, D2, D3, D4, D5, D6, D7, E2, E3, E4, E5, E6, E7, F2, F3, F4, F5, F6, F7, G2, G3, G4, G5, G6, H4, H5, H6, H7, H9, H10, H11	Input	**Radio System Ground.** Must be connected to RF Ground plane. Thermal relief required for proper soldering.
Dig_gnd_1 [1]	D12	Input	**Digital Ground**
Dig_gnd_2 [1]	G11	Input	**Digital Ground**
V_{CC}	H2	Input	**2.85V to 3.6V Input for Internal Power Supply Regulators**
VDD_ANA_OUT	J2	Output	**Voltage Regulator Output/Power Supply for Analog Circuitry.** If not used, place pad and do not connect to V_{CC} or Ground.
VDD_DIG_OUT	J5	Output	**Voltage Regulator Output/Power Supply for Digital Circuitry.** If not used, place pad and do not connect to V_{CC} or Ground.
VDD_DIG_PWR_D#	J4	Input	**Power Down for the Internal Power Supply Regulator for the Digital Circuitry.** Place pad and do not connect to V_{CC} or Ground.

1. Connect RF GND, Dig_gnd_1, and Dig_gnd_2 to a single ground plane.

6.0 Electrical Specifications

6.1 GENERAL SPECIFICATIONS

Absolute Maximum Ratings (see Table 9) indicate limits beyond which damage to the device may occur. Operating Ratings (see Table 10) indicate conditions for which the device is intended to be functional.

This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations.

The following conditions apply unless otherwise stated in the tables below:

- T_A = -40°C to +85°C
- V_{CC} = 3.3V, IOV_{CC} = 3.3V
- RF system performance specifications are guaranteed on National Semiconductor Austin Board rev1.0b reference design platform.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Logic Power Supply Voltage	-0.3	4.0	V
IOV_{CC}	I/O Power Supply Voltage	-0.3	4.0	V
USB_V_{CC} [1]	USB Power Supply Voltage	-0.5	3.63	V
V_I	Voltage on any pad with GND = 0V	-0.5	3.6	V
PinRF	RF Input Power		+15	dBm
T_S	Storage Temperature Range	-65	+125	^oC
T_L	Lead Temperature (solder 4 sec)		+235	^oC
ESD-HBM	ESD, Human Body Model		2000 [2]	V
ESD-MM	ESD, Machine Model		200	V
ESD-CDM	ESD, Charged Device Model		1000 [3]	V

1. USB Interface not supported by LMX9820A firmware. Treat as no connect. Pad required for mechanical stability.
2. Antenna pin passes 1500V HBM.
3. BRCLK(A12) pin passes 500V CDM.

Table 10. Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
V_{CC} [3]	Module Power Supply Voltage	2.85	3.3	3.6	V
IOV_{CC} [4]	I/O Power Supply Voltage	2.85	3.3	3.6	V
t_R	Module Power Supply Rise Time			50	ms
T_O	Operating Temperature Range	-40		+85	°C
HUM_{OP}	Humidity (operating, across operating temperature range)	10		90	%
HUM_{NONOP}	Humidity (non-operating, 38.7^{o}C web bulb temperature)	5		95	%

1. Maximum voltage difference allowed between V_{CC} and IOV_{CC} is 500 mV.
2. Typical operating conditions are V_{CC} = 3.3V, IOV_{CC} = 3.3V operating voltage and 25°C ambient temperature.
3. V_{CC} internally regulated to VDD_ANA (see Table 11)
4. IOV_{CC} internally regulated to VDD_DIG (see Table 11)

6.0 Electrical Specifications (Continued)

Table 11. Power Supply Electrical Specifications (Analog and Digital LDOs)

Symbol	Parameter	Min	Typ[1]	Max	Unit
VDD_ANA_OUT[2]	Analog Voltage Output Range		2.8		V
VDD_DIG_OUT[3]	Digital Voltage Output Range		2.5		V

1. Typical operating conditions are V_{CC} = 3.3V, IOV_{CC} = 3.3V operating voltage and 25°C ambient temperature. Values reflect voltages of internally generated, regulated voltages VDD_ANA and VDD_DIG
2. Output of internally generated regulated voltage VDD_ANA
3. Output of internally generated regulated voltage VDD_DIG

Note: The voltage regulators are optimized for the internal operation of the LMX9820A. Because any noise coupled into these supplies can have influence on the radio performance, it is highly recommended to have no additional load on their outputs.

Table 12. Power Supply Requirements[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
I_{CC-TX}	Power supply current for continuous transmit			68	mA
I_{CC-RX}	Power supply current for continuous receive			62	mA
I_{CC-Inq}	Inquiry		31		mA
I_{RXSL}	Receive Data in SPP Link, slave [3,4]		23		mA
I_{RXM}	Receive Data in SPP Link, master [3,4]		18		mA
I_{HV3}	Active HV3 SCO Audio Link		22		mA
I_{SnM}	Sniff Mode, sniff interval 1 second [3]		8		mA
$I_{SC-TLDIS}$	Scanning, no active link, TL disabled [3,5]		500		µA
I_{Idle}	Idle, scanning disabled, TL disabled [3,5]		150		µA

1. Power supply requirements based on Class II output power.
2. V_{CC} = 3.3V, IOV_{CC} = 3.3V, Ambient Temperature = +25°C.
3. Average values.
4. Based on UART Baudrate 115.2kbit/s.
5. TL: Transport Layer

6.0 Electrical Specifications (Continued)

6.2 DC CHARACTERISTICS

Table 13. Digital DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{CC}[1]	Core Logic Supply Voltage		2.85	3.6	V
IOV_{CC}[2]	IO Supply Voltage		2.85	3.6	V
V_{IH}	Logical 1 Input Voltage		0.7 x VDD_ANA	VDD_ANA + 0.5	V
V_{IL}	Logical 0 Input Voltage		-0.5	0.2 x VDD_ANA	V
V_{HYS}	Hysteresis Loop Width[3]		0.1 x VDD_ANA		V
I_{OH}	Logical 1 Output Current	VDD_ANA = 2.8V	-1.6		mA
I_{OL}	Logical 0 Output Current	VDD_ANA = 2.8V	1.6		mA
I_{OHW}	Weak Pull-up Current	VDD_ANA = 2.8V	-10		µA
I_{IH}	High-level Input Current	V_{IH} = VDD_ANA = 2.8V	- 10	10	µA
I_{IL}	Low-level Input Current	V_{IL} = 0	- 10	10	µA
I_L	High Impedance Input Leakage Current	$0V \le V_{IN} \le$ VDD_ANA	-2.0	2.0	µA
$I_{O(Off)}$	Output Leakage Current (I/O pins in input mode)	$0V \le V_{OUT} \le$ VDD_DIG	-2.0	2.0	µA

1. V_{CC} internally regulated to VDD_ANA (see Table 11)
2. IOV_{CC} internally regulated to VDD_DIG (see Table 11)
3. Guaranteed by design.

6.0 Electrical Specifications (Continued)

6.3 RF PERFORMANCE CHARACTERISTICS

In the performance characteristics tables the following applies:

- All tests performed are based on Bluetooth Test Specification rev 0.92.
- All tests are measured at antenna port unless otherwise specified
- T_A = -40°C to +85°C
- V_{CC} = 3.3V, IOV_{CC} = 3.3V unless otherwise specified

RF system performance specifications are guaranteed on National Semiconductor Austin Board rev1.0b reference design platform.

Table 14. Receiver Performance Characteristics

Symbol	Parameter	Condition		Min	Typ[1]	Max	Unit
RX_{sense} [2]	Receive Sensitivity	BER < 0.001	2.402 GHz		-81	-77	dBm
			2.441 GHz		-81	-77	dBm
			2.480 GHz		-81	-77	dBm
PinRF	Maximum Input Level			-10	0		dBm
C/I_{ACI} [3]	Carrier to Interferer Ratio in the Presence of Adjacent Channel Interferer	$\Delta F_{ACI} = \pm 1$ MHz, $P_{in}RF$ = -60 dBm, BER < 0.001				-1	dB
		$\Delta F_{ACI} = \pm 2$ MHz. $P_{in}RF$ = -60 dBm, BER < 0.001				-37	dB
		ΔF_{ACI} = + 3 MHz, $P_{in}RF$ = -67 dBm, BER < 0.001				-47	dB
C/I_{IMAGE} -1MHz	Carrier to Interferer Ratio in the Presence of Image-1MHz Interferer	Δf = -3 MHz, PinRF = -67 dBm, BER < 0.001				-32	dB
IMP[3,4]	Intermodulation Performance	F_1= + 3 MHz, F_2= + 6 MHz, $P_{in}RF$ = -64 dBm		-38	-36		dBm
RSSI	RSSI Dynamic Range at LNA Input			-72		-52	dBm
Z_{RFIN}	Input Impedance of RF Port (RF_inout)	Single input impedance F_{in} = 2.45 GHz			50		Ω
Return Loss[3]	Return Loss					-8	dB
OOB[3]	Out Of Band Blocking Performance	$P_{in}RF$ = -10 dBm, 30 MHz < F_{CWI} < 2 GHz, BER < 0.001		-10			dBm
		$P_{in}RF$ = -27 dBm, 2000 MHz < F_{CWI} < 2399 MHz, BER < 0.001		-27			dBm
		$P_{in}RF$ = -27 dBm, 2498 MHz < F_{CWI} < 3000 MHz, BER < 0.001		-27			dBm
		$P_{in}RF$ = -10 dBm, 3000 MHz < F_{CWI} < 12.75 GHz, BER < 0.001		-10			dBm

1. Typical operating conditions are at 2.85V operating voltage and 25°C ambient temperature.
2. The receiver sensitivity is measured at the device interface.
3. Not tested in production.
4. The f_0 = -64 dBm Bluetooth modulated signal, f_1 = -39 dbm sine wave, f_2 = -39 dBm Bluetooth modulated signal, $f_0 = 2f_1 - f_2$, and $|f_2 - f_1|$ = n x 1 MHz, in which n is 3, 4, or 5. For the typical case, n = 3.

6.0 Electrical Specifications (Continued)

Table 15. Transmitter Performance Characteristics

Symbol	Parameter	Condition	Min	Typ[1]	Max	Unit
$P_{OUT}RF$ [2]	Transmit Output Power	2.402 GHz	-3	+1	+4	dBm
		2.441 GHz	-3	+1	+4	dBm
		2.480 GHz	-3	+1	+4	dBm
Power Density [5]	Power Density		-4	1	2	dBm
MOD $\Delta F1_{AVG}$	Modulation Characteristics	Data = 00001111	140	165	175	kHz
MOD $\Delta F2_{MAX}$ [3]	Modulation Characteristics	Data = 10101010	115	125		kHz
$\Delta F2_{AVG}/\Delta F1_{AVG}$ [4]	Modulation Characteristics		0.8			
20 dB Bandwidth					1000	kHz
ACP [5]	Adjacent Channel Power (In-band Spurious)	| M - N | = 2		-48	-20	dBm
		| M - N | $\geq$ 3		-51	-40	dBm
$P_{OUT}2*f_o$ [6]	PA 2nd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 4804 MHz			-30	dBm
$P_{OUT}3*f_o$ [5]	PA 3rd Harmonic Suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 7206 MHz			-32	dBm
Z_{RFOUT}	RF Output Impedance/Input Impedance of RF Port (RF_inout)	P_{out} @ 2.5 GHz		50		Ω
Return Loss [5]	Return Loss				-14	dB

1. Typical operating conditions are at V_{CC} = 3.3V, IOV_{CC} = 3.3V operating voltage and 25°C ambient temperature.
2. The output power is measure at the device interface.
3. ΔF2max > 115 kHz for at least 99.9% of all Δf2max.
4. Modulation index set between 0.28 and 0.35.
5. Not tested in production.
6. Out-of-Band spurs only exist at 2nd and 3rd harmonics of the CW frequency for each channel.

Table 16. Synthesizer Performance Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO Frequency Range			5000		MHz
t_{LOCK}	Lock Time	$f_0 \pm$ 20 kHz		120		µs
Δf_0offset [1,2]	Initial Carrier Frequency Tolerance	During preamble	-75	0	75	kHz
Δf_0drift [2,3]	Initial Carrier Frequency Drift	DH1 data packet	-25	0	25	kHz
		DH3 data packet	-40	0	40	kHz
		DH5 data packet	-40	0	40	kHz
		Drift Rate	-20	0	20	kHz/50µs
t_D-Tx	Transmitter Delay Time	From Tx data to antenna		4		µs

1. Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of <20 ppm to meet Bluetooth specifications.
2. Not tested in production.
3. Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of <20 ppm to meet Bluetooth specifications.

6.0 Electrical Specifications (Continued)

6.4 PERFORMANCE DATA (TYPICAL)

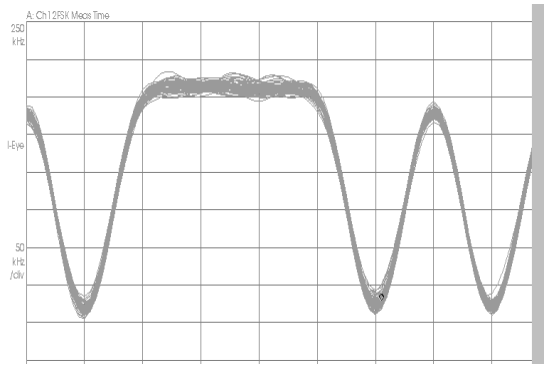


Figure 2. Modulation

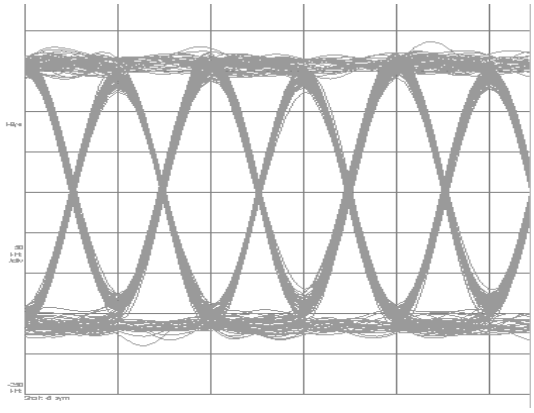


Figure 4. Corresponding Eye Diagram

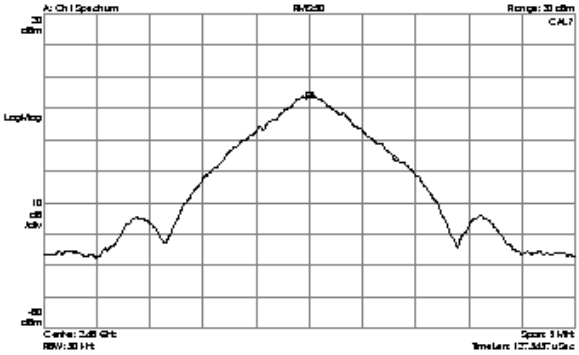


Figure 3. Transmit Spectrum

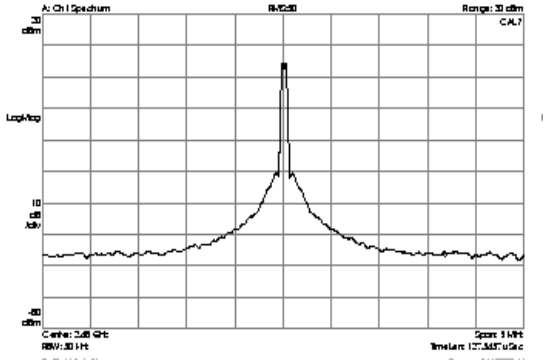


Figure 5. Synthesizer Phase Noise

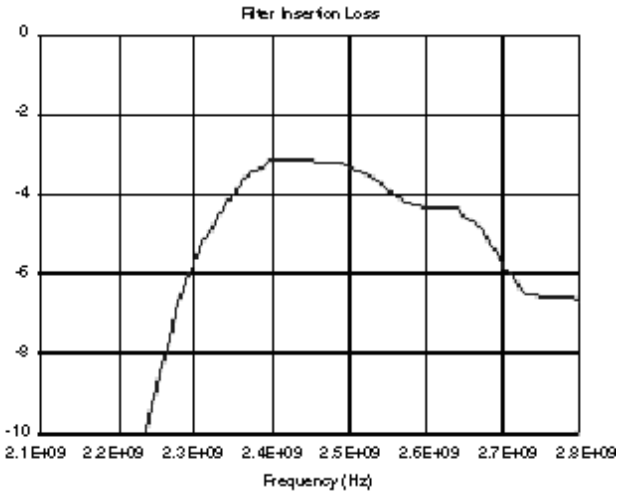


Figure 6. Front-End Bandpass Filter Response

6.0 Electrical Specifications (Continued)

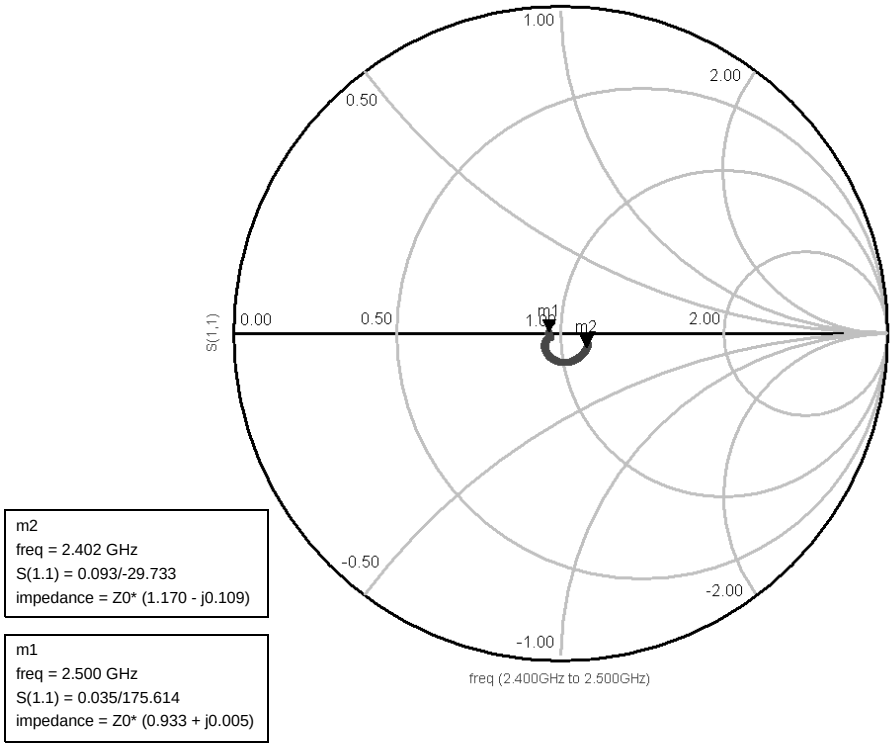


Figure 7. TX and RX Pin 50Ω Impedance Characteristics

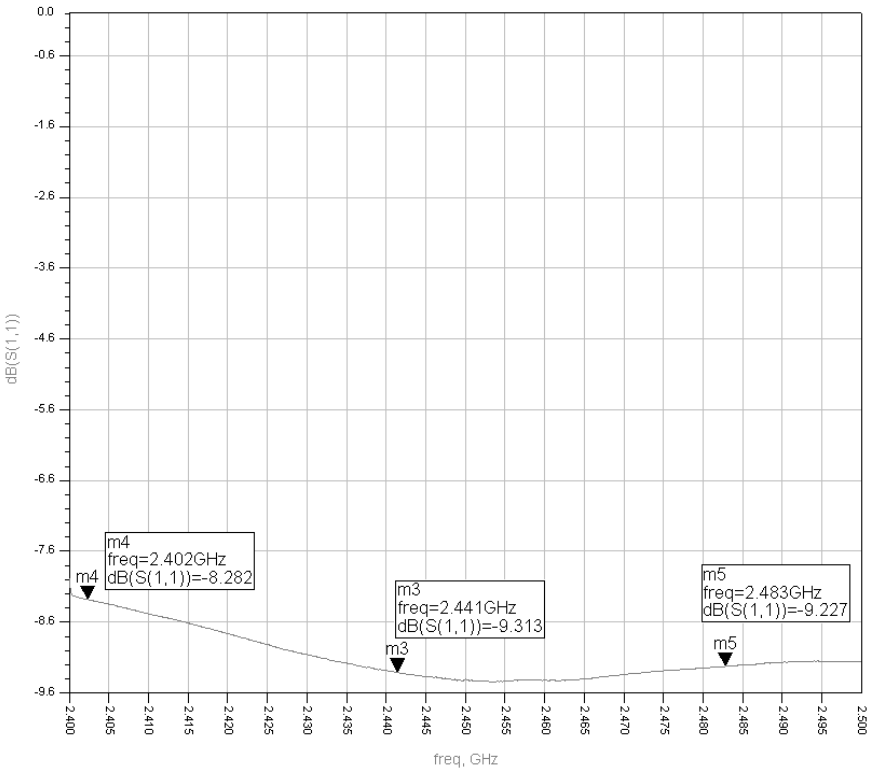


Figure 8. Transceiver Return Loss

7.0 Functional Description

7.1 BASEBAND AND LINK MANAGEMENT PROCESSORS

Baseband and Lower Link control functions are implemented using a combination of National Semiconductor's CompactRISC 16-bit processor and the Bluetooth Lower Link Controller. These processors operate from integrated Flash memory and RAM and execute on-board firmware implementing all Bluetooth functions.

7.1.1 Bluetooth Lower Link Controller

The integrated Bluetooth Lower Link Controller (LLC) complies with the Bluetooth Specification version 1.1 and implements the following functions:

- Support for 1, 3, and 5 slot packet types
- 79-channel hop frequency generation circuitry
- Fast frequency hopping at 1600 hops per second
- Power management control
- Access code correlation and slot timing recovery

7.1.2 Bluetooth Upper Layer Stack

The integrated upper layer stack is prequalified and includes the following protocol layers:

- L2CAP
- RFComm
- SDP

7.1.3 Profile Support

The on-chip application of the LMX9820A allows full standalone operation, without any Bluetooth protocol layer necessary outside the module. It supports the Generic Access Profile (GAP), the Service Discovery Application Profile (SDAP), and the Serial Port Profile (SPP).

The on-chip profiles can be used as interfaces to additional profiles executed on the host. The LMX9820A includes a configurable service database to answer requests with the profiles supported.

7.1.4 Application with Command Interface

The module supports automatic slave operation eliminating the need for an external control unit. The implemented transparent option enables the chip to handle incoming data raw, without the need for packaging in a special format. The device uses a fixed pin to block unallowed connections.

Acting as master, the application offers a simple but versatile command interface for standard Bluetooth operations such as inquiry, service discovery, and serial port connection. The firmware supports up to three slaves. Default Link Policy settings and a specific master mode allow optimized configuration for the application specific requirements. See also Section "Integrated Firmware" on page 24.

7.2 MEMORY

The LMX9820A includes 256KB of programmable Flash memory that can be used for code and constant data. It allows single-cycle read access from the CPU. In addition to storing all algorithms and firmware, the on-board Flash also contains the IEEE 802 compliant Media Access Controller (MAC) address (BDADDR). The firmware and the BDADDR are programmed by National Semiconductor or can be programmed by the customer either before assembly into the host system or in-system. Module firmware can also be updated during manufacturing or in-system using the ISP capabilities of the LMX9820A. The LMX9820A firmware uses the internal RAM for buffers and program variables.

7.3 CONTROL AND TRANSPORT PORT

The LMX9820A provides one Universal Asynchronous Receiver Transmitter (UART). It supports 8-bit data formats with or without parity and one or two stop bits. The baud rate is generated by hardware that is programmed at boot time. Alternatively, the speed and configuration settings can be read out of internal memory settings. The UART can operate at baud rates of 2.4k, 4.8k, 7.2k, 9.6k, 19.2k, 38.4k, 57.6k, 115.2k, 230.4k, 460.8k and 921.6k. It implements flow control logic (RTS, CTS) to provide hardware handshaking capability. The UART offers wakeup from the low-power modes through the multi-input wakeup module. UART logic thresholds are set via the IOV_{CC} pin.

7.4 AUXILIARY PORTS

7.4.1 Reset_5100 and Reset_b#

Reset_5100 and Reset_b# are active low reset inputs for the baseband controller and digital smart radio portions of the LMX9820A, respectively. These pins are normally tied together and are connected to the host system so that the host can initialize the LMX9820A by asserting the reset inputs. Upon de-assertion, the status of the module operating environment (Env) pads are sampled and the LMX9820A enters the corresponding operational mode.

7.4.2 Operating Environment Pads (Env0 and Env1)

The module provides two operating environments (see Table 17) selected by the states on the Env inputs sampled at reset.

The ISP mode allows end-of-line or field programming of the LMX9820A Flash memory by starting the baseband controller from the boot block of memory.

Table 17. Operating Environments

Operating Environment	Env1 (Pad B11)	Env0 (Pad E9)
ISP Mode	1	0
Run (Normal) Mode (Default)	1	1

7.0 Functional Description (Continued)

7.4.3 Interface Select Inputs (ISEL1, ISEL2)

The interface selection pads are used for setting the UART speed and settings. If ISEL1 and ISEL2 are unconnected, they are pulled high by weak internal pullups, which select a default baudrate of 921.6k baud. The settings for Stopbits, Startbit, and Parity are stored as internal non-volatile storage (NVS) parameters. If a baud rate different from the values listed in Table 18 is needed, ISEL 1 and ISEL2 must be pulled low. This forces the device to read the UART speed from the parameter table in NVS. The default baud rate value programmed in NVS is 9.6k baud, however the device firmware can be modified to support other values. The default configuration in NVS is 1 Stopbit, 1 Startbit, and No parity. Table 18 shows the ISEL1 and ISEL2 selection settings.

Table 18. UART Speed Selection

ISEL1 (Pad J13)	ISEL2 (Pad H13)	Interface Speed (baud)	UART Settings
1	1	921.6k	From NVS
0	1	115.2k	From NVS
1	0	9.6k	1Stop, 1Start, No Parity
0	0	Check NVS	From NVS

7.4.4 Module and LInk Status Outputs

The LMX9820A provides signals that the host can use to determine the real-time status of the radio link. The TX_Switch_P signal (pad H3) is a real-time indication of the current configuration (direction) of the transceiver. The link status lines (Lstat_0 and Lstat_1, pads E8 and F8, respectively) are GPIO lines controlled by the LMX9820A firmware. The Host Wakeup line (Host_wu, pad F9) is implemented using GPIO and firmware. It is used to bring the host processor out of Sleep mode when link activity calls for host processing. Host_wu can also be used by the host to check if link activity is present. If Host_wu is active, then link activity is present and the host loses network awareness if the operating system continues to allow the host processor to enter Sleep mode. Table 19 presents the definitions of the various module and link status outputs.

Table 19. Module/Link Status Definitions

Lstat_0 (Pad E8)	Lstat_1 (Pad F8)	TX_Switch_P (Pad H3)	Host_wu (Pad F9)	Mode
x	1	x	x	At least 1 SPP link established
x	0	x	x	No active SPP link
x	x	1	x	Transceiver = Transmit
x	x	0	x	Transceiver = Receive
x	x	x	0	Host can Sleep
x	x	x	1	Wakeup host/host should not Sleep

7.5 AUDIO PORT

Advanced Audio Interface

The Advanced Audio Interface (AAI) is an advanced version of the Synchronous Serial Interface (SSI) that provides a full-duplex communications port to a variety of industry-standard 13/14/15/16-bit linear or 8-bit log PCM codecs, DSPs, and other serial audio devices.

The LMX9820A allows the support for one codec. The firmware selects the desired audio path and interface configuration by a parameter stored in NVS. The audio path options include the Motorola MC145483 codec, OKI MSM7717 codecs, and the PCM slave through the AAI, or no audio.

Table 20 summarizes the audio path selection and the configuration of the audio interface at the specific mode.

Table 20. Audio Path Configuration

Audio Path	Format	AAI Bit Clock	AAI Frame Clock	AAI Frame Sync Pulse Length
Motorola MC145483[1]	13-bit linear	480 kHz	8 kHz	13 bits
OKI MSM7717	8-bit log PCM (A-law only)	120 kHz	8 kHz	14 bits
PCM slave[2]	8/16 bits	128 - 1024 KHz	8 kHz	8/16 bits

1. Due to internal clock divider limitations, the optimum of 512 kHz, 8 kHz cannot be reached. The values are set to the best possible values. The clock mismatch does not result in any discernible loss in audio quality.
2. In PCM slave mode, parameters are stored in NVS. Bit clock and frame clock must be generated by the host interface.

8.0 Digital Smart Radio

8.1 FUNCTIONAL DESCRIPTION

The integrated Digital Smart Radio uses a heterodyne receiver architecture with a low intermediate frequency (2 MHz), such that the intermediate frequency filters can be integrated on-chip. The receiver consists of a low-noise amplifier (LNA) followed by two mixers. The intermediate frequency signal processing blocks consist of a poly-phase bandpass filter (BPF), two hard limiters (LIM), a frequency discriminator (DET), and a post-detection filter (PDF). The received signal level is detected by a received signal strength indicator (RSSI).

The received frequency equals the local oscillator frequency (fLO) plus the intermediate frequency (fIF):

fRF = fLO + fIF (supradyne).

The radio includes a synthesizer consisting of a phase detector, a charge pump, an (off-chip) loop filter, an RF frequency divider, and a voltage-controlled oscillator (VCO).

The transmitter uses IQ-modulation with bit-stream data that is gaussian filtered. Other blocks included in the transmitter are a VCO buffer and a power amplifier (PA).

8.2 RECEIVER FRONT END

The receiver front end consists of a low-noise amplifier (LNA) followed by two mixers and two low-pass filters for the I- and Q-channels.

The intermediate frequency (IF) part of the receiver front end consists of two IF amplifiers that receive input signals from the mixers, delivering balanced I- and Q-signals to the poly-phase bandpass filter. The poly-phase bandpass filter is directly followed by two hard limiters that together generate an AD-converted RSSI signal.

8.2.1 Poly-Phase Bandpass Filter

The purpose of the IF bandpass filter is to reject noise and spurious (mainly adjacent channel) interference that would otherwise enter the hard-limiting stage. In addition, it handles image rejection.

The bandpass filter uses both the I- and Q-signals from the mixers. The out-of-band suppression should be higher than 40 dB (f < 1 MHz, f > 3 MHz). The bandpass filter is tuned over process spread and temperature variations by the autotuner circuitry. A 5th-order Butterworth filter is used.

8.2.2 Hard Limiter and RSSI

The I- and Q-outputs of the bandpass filter are each followed by a hard-limiter. The hard-limiter has its own reference current. The RSSI (Received Signal Strength Indicator) reports the level of the RF input signal.

The RSSI is generated by piece-wise linear approximation of the level of the RF signal. The RSSI has a mV/dB scale, and an analog-to-digital converter for processing by the baseband circuit. The input RF power is converted to a 5-bit value. The RSSI value is then proportional to the input power (in dBm).

The digital output from the ADC is sampled on the BPKTCTL signal low-to-high transition.

8.3 RECEIVER BACK END

The hard limiters are followed by two frequency discriminators. The I-frequency discriminator uses the 90^o phase-shifted signal from the Q-path, while the Q-discriminator uses the 90^o phase-shifted signal from the I-path. A poly-phase bandpass filter performs the required phase shifting. The output signals of the I- and Q-discriminator are subtracted and filtered by a low-pass filter. An equalizer is added to improve the eye-pattern for 101010 patterns.

After equalization, a dynamic AFC (automatic frequency offset compensation) circuit and slicer extract the RX_DATA from the analog data pattern. The Eb/No of the demodulator is approximately 17 dB.

8.3.1 Frequency Discriminator

The frequency discriminator gets its input signals from the limiter. A defined signal level (independent of the power supply voltage) is needed to obtain the input signal. Both inputs of the frequency discriminator have limiting circuits to optimize performance. The bandpass filter in the frequency discriminator is tuned by the autotuning circuitry.

8.3.2 Post-Detection Filter and Equalizer

The output signals of the FM discriminator go through a post-detection filter followed by an equalizer. Both the post-detection filter and equalizer are tuned to the proper frequency by the autotuning circuitry. The post-detection filter is a low-pass filter intended to suppress all remaining spurious signals, such as the second harmonic (4 MHz) from the FM detector and noise generated after the limiter.

The post-detection filter also helps for attenuating the first adjacent channel signal. The equalizer improves the eye-opening for 101010 patterns. The post-detection filter is a third-order Butterworth filter.

8.4 AUTOTUNING CIRCUITRY

The autotuning circuitry is used for tuning the bandpass filter, detector, post-detection filter, equalizer, and transmit filters for process and temperature variations. The circuitry includes offset compensation for the FM detector.

8.5 SYNTHESIZER

The synthesizer consists of a phase-frequency detector, a charge pump, a low-pass loop filter, a programmable frequency divider, a voltage-controlled oscillator (VCO), a delta-sigma modulator, and a lookup table.

The frequency divider consists of a divide-by-2 circuit (divides the 5 GHz signal from the VCO down to 2.5 GHz), a divide-by-8-or-9 divider, and a digital modulus control. The delta-sigma modulator controls the division ratio and also generates an input channel value to the lookup table.

8.5.1 Phase-Frequency Detector

The phase-frequency detector is a 5-state phase-detector. It responds only to transitions, hence phase-error is independent of input waveform duty cycle or amplitude variations. Loop lockup occurs when all the negative transitions on the inputs, F_REF and F_MOD, coincide. Both outputs (i.e., Up and Down) then remain high. This is equal to the zero error mode. The phase-frequency detector input frequency range operates at 12 MHz.

8.0 Digital Smart Radio (Continued)

8.6 TRANSMITTER CIRCUITRY

The transmitter consists of ROM tables, two Digital to Analog (DA) converters, two low-pass filters, IQ mixers, and a power amplifier (PA).

The ROM tables generate a digital IQ signal based on the transmit data. The output of the ROM tables is inserted into IQ-DA converters and filtered through two low-pass filters. The two signal components are mixed up to 2.5 GHz by the TX mixers and added together before being inserted into the transmit PA.

8.6.1 IQ-DA Converters and TX Mixers

The ROM output signals drive an I- and Q-DA converter. Two Butterworth low-pass filters filter the DA output signals. The 6 MHz clock for the DA converters and the logic circuitry around the ROM tables are derived from the autotuner.

The TX mixers mix the balanced I- and Q-signals up to 2.4-2.5 GHz. The output signals of the I- and Q-mixers are summed.

8.7 CRYSTAL REQUIREMENTS

The LMX9820A includes a crystal driver circuit. This circuit operates with an external crystal and capacitors to form an oscillator. Figure 9 shows the recommended crystal circuit. Table 24 on page 22 specifies system clock requirements.

The RF local oscillator and internal digital clocks for the LMX9820A are derived from the reference clock at the CLK+ input. This reference may either come from an external clock or a dedicated crystal oscillator. The crystal oscillator connections require a crystal and two grounded capacitors.

It is important to consider board- and design-dependent capacitance in tuning the crystal circuit. The following equations allow a close approximation of the required crystal tuning capacitance, but the actual values will vary with the capacitive properties of the board. As a result, there is some fine tuning of the crystal circuit which cannot be calculated, but must be determined experimentally by testing different values of load capacitance.

Many different crystals can be used with the LMX9820A. A key requirement from the Bluetooth specification is 20 ppm. Additionally, ESR (Equivalent Series Resistance) must be carefully considered. LMX9820A can support a maximum of 230Ω ESR, but it is recommended to stay < 100Ω ESR for best performance over voltage and temperature. See Figure 14 on page 22 for ESR as part of the crystal circuit for more information.

8.7.1 Crystal

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

1. Load Capacitance

For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance, which is the value of capacitance used in conjunction with the crystal unit. Load capacitance is a parameter specified by the crystal, typically expressed in pF. The crystal circuit shown in Figure 10 on page 19 is composed of:

— C1 (motional capacitance)

— R1 (motional resistance)

— L1 (motional inductance)

— C0 (static or shunt capacitance)

The LMX9820A provides some of the load with internal capacitors C_{int}. The remainder must come from the external capacitors and tuning capacitors labeled Ct1 and Ct2 as shown in Figure 9. Ct1 and Ct2 should have the same the value for best noise performance.

The LMX9820A has an additional internal capacitance C_{TUNE} of 2.6 pF. Crystal load capacitance ($C_{L)}$ is calculated as:

$C_L = C_{int} + C_{TUNE} + Ct1/Ct2$

The C_L above does not include the crystal internal self-capacitance C_0 as shown in Figure 10 on page 19, so the total capacitance is:

$C_{total} = C_L + C_0$

Based on the crystal specification and equation:

$C_L = C_{int} + C_{TUNE} + Ct1//Ct2$

$C_L = 8pF + 2.6pF + 6pF = 16.6pF$

16.6 pF is very close to the TEW crystal requirement of 16 pF load capacitance. With the internal shunt capacitance C_{total}:

$C_{total} = 16.6pF + 5pF = 21.6pF$

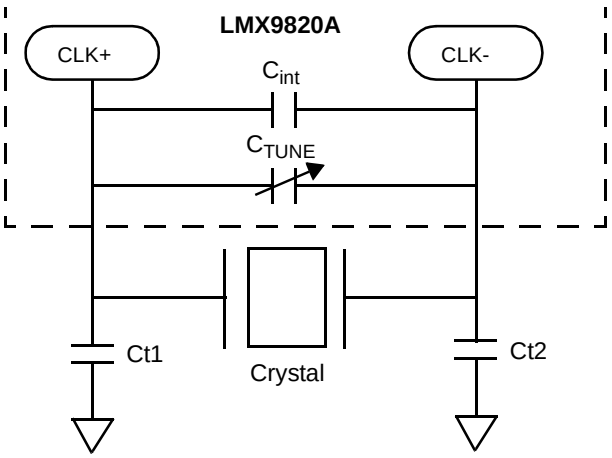


Figure 9. LMX9820A Crystal Recommended Circuit

8.0 Digital Smart Radio (Continued)

2. Crystal Pullability

Pullability is another important parameter for a crystal, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

3. Frequency Tuning

Frequency tuning is achieved by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within 20 ppm. The crystal network or oscillator must have cumulative accuracy specifications of **15 ppm** to provide margin for frequency drift with aging and temperature.

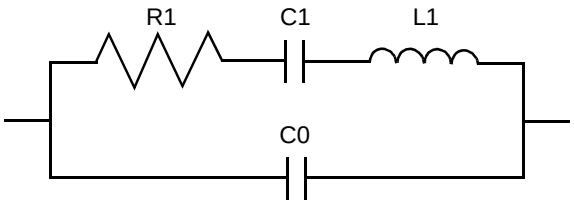


Figure 10. Crystal Equivalent Circuit

TEW Crystal

The LMX9820A has been tested with the TEW TAS-4025A crystal, see Table 21 on page 19 for specification. Because the internal capacitance of the crystal circuit is 8 pF and the load capacitance is 16 pF, 12 pF is a good starting point for both Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. Figure 11 on page 20 shows the RF frequency offset test results.

Figure 11 on page 20 shows the results are -20 kHz off the center frequency, which is -1 ppm. The pullability of the crystal is 2 ppm/pF, so the load capacitance must be decreased by about 1.0 pF. By changing Ct1 or Ct2 to 10 pF, the total load capacitance is decreased by 1.0 pF. Figure 12 on page 20 shows the frequency offset test results. The frequency offset is now zero with Ct1 = 10 pF, Ct2 = 10 pF.

Reference Table 22 on page 19 for crystal tuning values used on Austin Development Board with TEW crystal.

Table 21. TEW TAS-4025A

Specification	Value
Package	4.0 x 2.5 x 0.65 mm (4 pads)
Frequency	12.000 MHz
Mode	Fundamental
Stability	>15 ppm @ -40 to +85°C
C_L Load Capacitance	16 pF
ESR	80Ω max.
C_0 Shunt Capacitance	5 pF
Drive Level	50 ±10uV
Pullability	2 ppm/pF min
Storage Temperature	-40 to +85°C

Table 22. TEW on Arizona Board

Reference	LMX9820A
Ct1	10 pF
Ct2	10 pF

8.0 Digital Smart Radio (Continued)

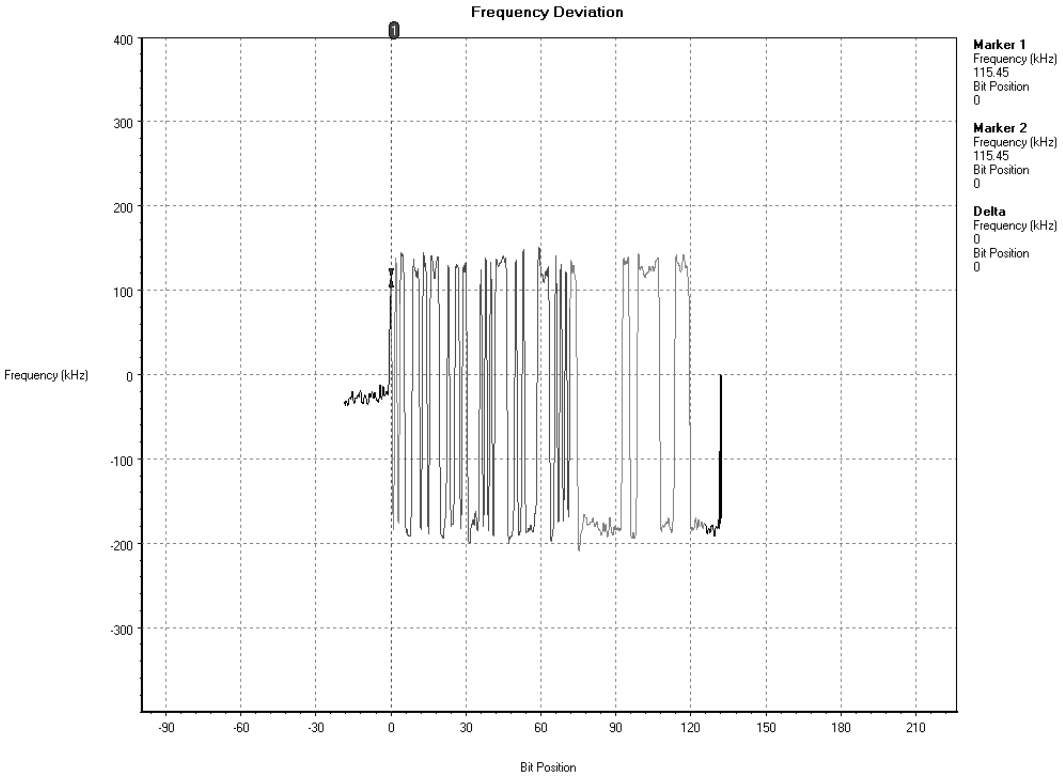


Figure 11. Frequency Offset with 12 pF/12 pF Capacitors

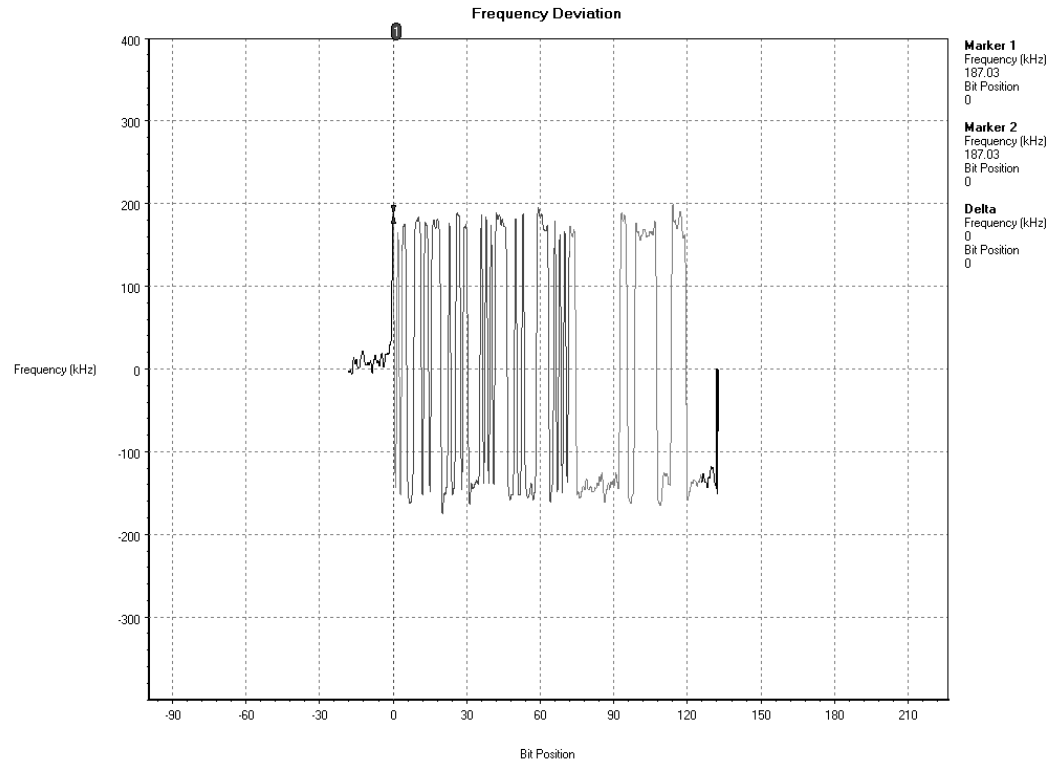


Figure 12. Frequency Offset with 10 pF/10 pF Capacitors

8.0 Digital Smart Radio (Continued)

8.7.2 TCXO (Temperature Compensated Crystal Oscillator)

The LMX9820A also can operate with an external TCXO (Temperature Compensated Crystal Oscillator). The TCXO signal is directly connected to the CLK+.

1. Input Impedance

The LMX9820A CLK+ pin has in input impedance of 2 pF capacitance in parallel with >400kΩ resistance.

8.7.3 Optional 32 kHz Oscillator

A second oscillator is provided (see Figure 13) that is tuned to provide optimum performance and low-power consumption while operating with a 32.768 kHz crystal. An external crystal clock network is required between the 32kHz_CLKI clock input (pad B13) and the 32kHz_CLKO clock output (pad C13) signals.The oscillator is built in a Pierce configuration and uses two external capacitors. Table 23 provides the oscillator's specifications.

In case the 32Khz is placed optionally, it is recommended to remove C2 and replace C1 with a zero ohm resistor.

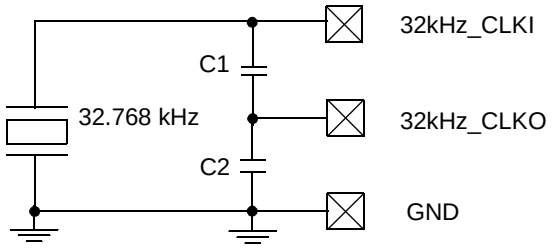


Figure 13. 32.768 kHz Oscillator

Table 23. 32.768 kHz Oscillator Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.62	1.8	1.98	V
I_{DDACT}	Supply Current (Active)			2		µA
f	Nominal Output Frequency			32.768		kHz
V_{PPOSC}	Oscillating Amplitude			1.8		V
	Duty Cycle		40		60	%

8.0 Digital Smart Radio (Continued)

8.7.4 ESR (Equivalent Series Resistance)

LMX9820A can operate with a wide range of crystals with different ESR ratings. Reference Table 24 on page 22 and Figure 14 on page 22 for more details.

Table 24. System Clock Requirements

Parameter	Min	Typ	Max	Unit
External Reference Clock Frequency		12 MHz		MHz
Frequency Tolerance (over full operating temperature and aging)		15	20	ppm
Crystal Serial Resistance			230	Ω
External Reference Clock Power Swing, pk to pk	100	200	400	mV
Aging			1	ppm per year

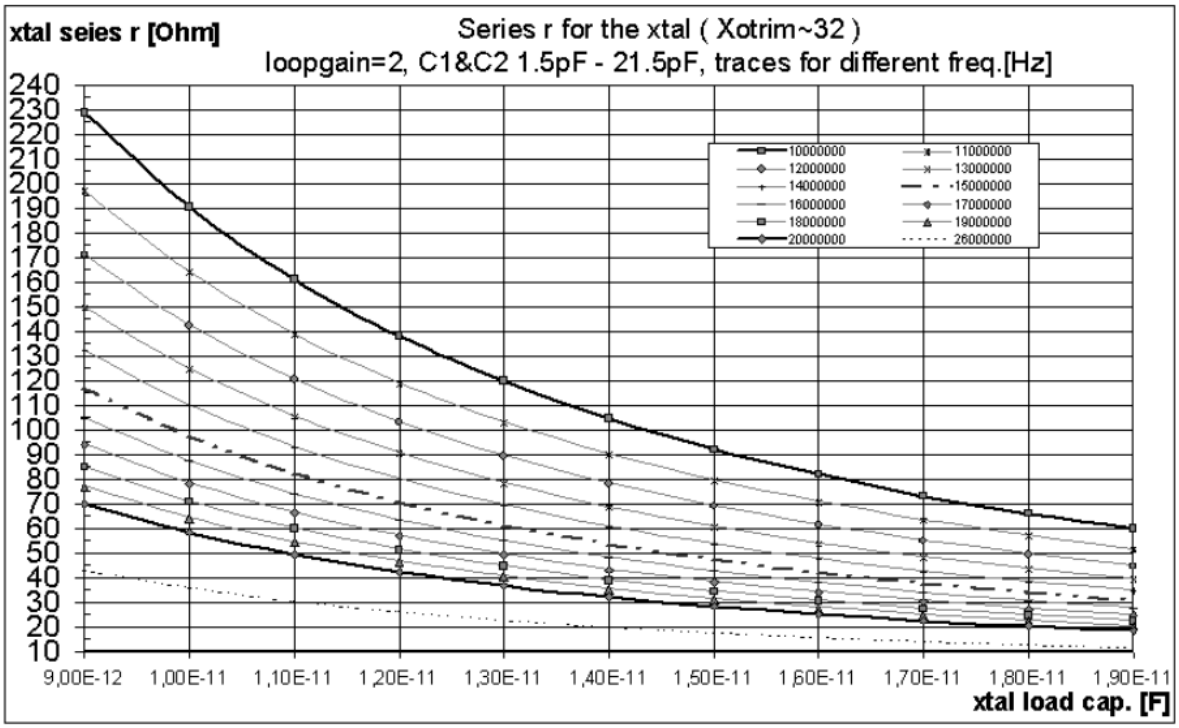


Figure 14. ESR vs. Load Capacitance for the Crystal

8.8 ANTENNA MATCHING AND FRONT-END FILTERING

Figure 15 shows the recommended component layout to be used between RF output and antenna input. Allows for versatility in the design such that the match to the antenna maybe improved and/or the blocking margin increased by addition of a LC filter. Refer to antenna design application note rev1.1 for further details

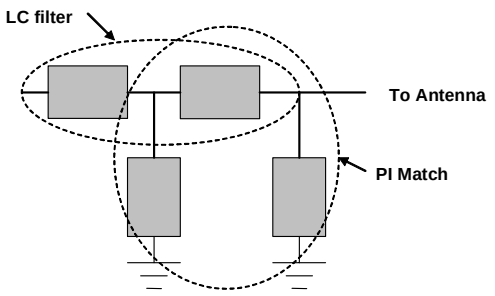


Figure 15. Front End Layout

9.0 System Power-Up Sequence

The following sequence must be performed to correctly power-up the LMX9820A:

1. Apply IOV_{CC} and V_{CC} to the LMX9820A.
2. Reset_b# and Reset_5100# of the LMX9820A are driven high a minimum of 2 ms after the LMX9820A voltage rails are high. The LMX9820A is the properly reset.

See Table 25 on page 23.

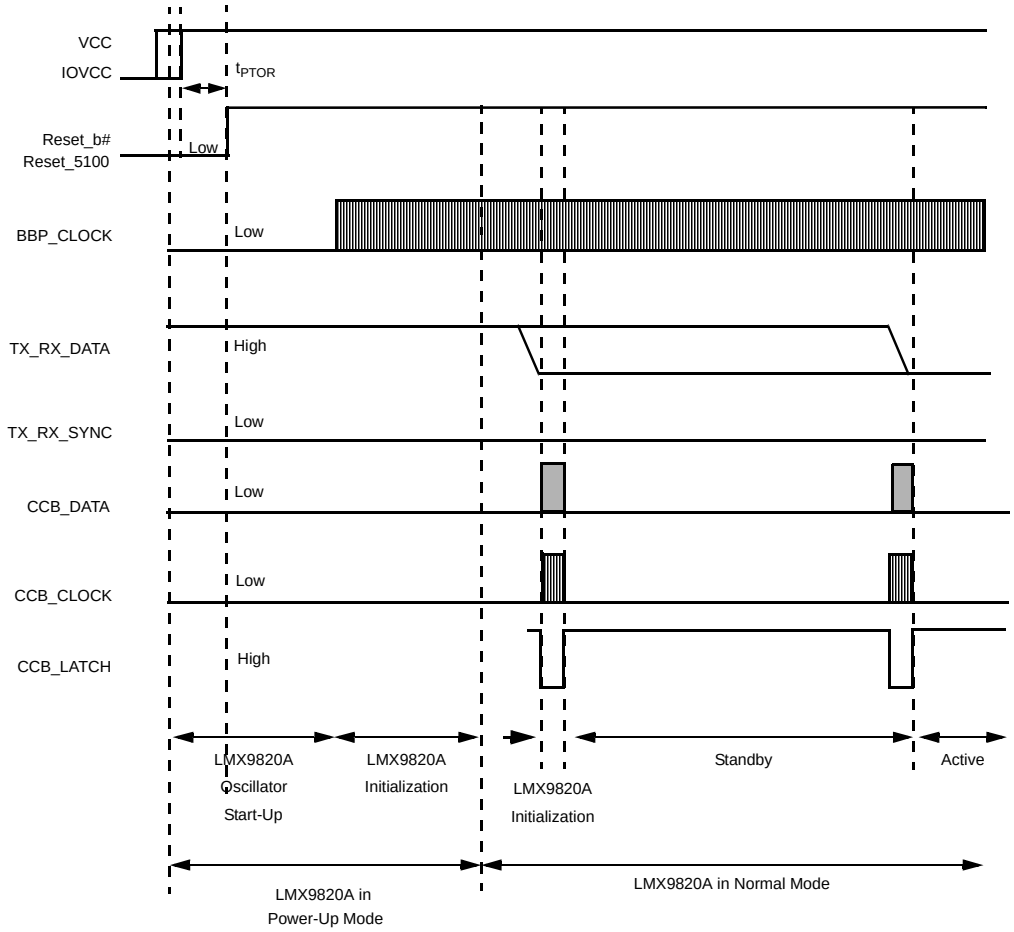


Figure 16. LMX9820A System Power-Up Sequence Timing

Table 25. LMX9820A System Power-up Sequence Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PTOR}	Power to Reset	V_{CC} and IOV_{CC} at operating voltage level to valid reset	2			ms

10.0 Integrated Firmware

The LMX9820A includes the full Bluetooth protocol stack up to RFComm to support the following profiles:

— GAP (Generic Access Profile)

— SDAP (Service Discovery Application Profile)

— SPP (Serial Port Profile)

Figure 17 shows the Bluetooth protocol stack with command interpreter interface. The command interpreter offers a number of different commands to support the functionality given by the different profiles. Execution and interface timing is handled by the control application.

The chip has an internal data area in Flash and the NVS parameters can be found in the Software Users Guide.

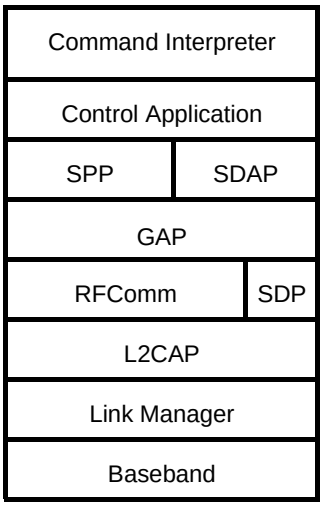


Figure 17. LMX9820A Software Implementation

10.1 FEATURES

10.1.1 Operation Modes

On boot-up, the application configures the module following the parameters in the data area.

Automatic Mode

No Default Connections Stored

In Automatic mode the module is connectable and discoverable and automatically answers to service requests. The command interpreter listens to commands and links can be set up. The full command list is supported.

If connected by another device, the module sends an event back to the host, where the RFComm port has been connected, and switches to transparent mode.

Default Connections Stored

If default connections were stored on a previous session, after the LMX9820A is reset, it will attempt to reconnect to each device stored within the data Flash three times. The host will be notified about the success of the link setup via a link status event.

Command Mode

In Command mode, the LMX9820A does not check the default connections section within the Data Flash. If connected by another device, it will *not* switch to transparent mode and continue to interpret data sent on the UART.

Transparent Mode

The LMX9820A supports transparent data communication from the UART interface to a Bluetooth link.

If activated, the module does not interpret the commands on the UART which normally are used to configure and control the module. In this case, the packets do not need to be formatted as described in Table 27 on page 27. Instead, all data are directly passed through the firmware to the active Bluetooth link and the remote device.

Transparent mode can only be supported on a point-to-point connection. To leave Transparent mode, the host must send a UART_BREAK signal to the module

Force Master Mode

In Force Master mode, the LMX9820A tries to act like an Access point for multiple connections. In this mode, it will only accept a link if a master/slave role switch is accepted by the connecting device. After successful link establishment, the LMX9820A will be master and available for additional incoming links. On the first incoming link the LMX9820A may switch to transparent mode, depending on the setting for automatic or command mode. Additional links will only be possible if the device is not in transparent mode.

10.1.2 Default Connections

The LMX9820A supports the storage of up to 3 default connections within its NVS. Those connections can either be connected after reset or on demand using a specific command.

10.1.3 Event Filter

The LMX9820A uses events or indicators to notify the host about successful commands or changes on the Bluetooth interface. Depending on the application, the LMX9820A can be configured. The following levels are defined:

- *No Events*—the LMX9820A is not reporting any events. Optimized for passive cable replacement solutions.
- *Standard LMX9820A Events*—only necessary events will be reported.
- *All Events*—additional to the standard all changes at the physical layer will be reported.

10.1.4 Default Link Policy

Each Bluetooth link can be configured to support master/slave role switch, Hold mode, Sniff mode, and Park mode. The default link policy defines the standard setting for incoming and outgoing connections.

10.1.5 Audio Support

The LMX9820A offers commands to establish and release synchronous connections (SCO) to support Headset or Handsfree applications. The firmware supports one active link with all available package types (HV1, HV2, HV3), for routing audio data between the Bluetooth link and the advanced audio interface. To provide the analog data interface, an external audio codec is required. The LMX9820A includes a list of codecs which can be used

10.1.6 Default Sniff operation

To support optimized power consumption, the LMX9820A offers the ability to enable Sniff mode during link establishment on incoming links or on default connection setup. The default parameters for the Sniff mode are stored in NVS.

11.0 Power Reduction

The LMX9820A supports several low-power modes to reduce power in different operating situations. The modular structure of the LMX9820A allows the firmware to power down unused modules.

The low-power modes have influence on:

- *UART transport layer*—enables or disables the interface.
- *Bluetooth Baseband activity*—firmware disables LLC and radio, if possible.

11.1 LOW POWER MODES

The following LMX9820A power modes, which depend on the activity level of the UART transport layer and the radio activity, are defined:

The activity of the Bluetooth radio mainly depends on application requirements and is controlled by standard Bluetooth operations such as inquiry/page scanning or an active link. A remote device establishing or disconnecting a link may also indirectly change the activity level of the radio.

The UART transport layer by default is enabled on device power up. The “Disable Transport Layer” command is used to disable the transport layer. Therefore, only the host-side command interface can disable the transport layer. Enabling the transport layer is controlled by the hardware wake-up signalling. This can be initiated from either the host or an LMX9820A input. See also “LMX9820A Software Users Guide” for detailed information on timing and implementation requirements.

Table 26. Power Mode Activity

Power Mode	UART	Bluetooth Radio	Reference Clock
PM0	Off	Off	None
PM1	On	Off	12 MHz
PM2	Off	Scanning	12 MHz / 32kHz[1]
PM3	On	Scanning	12 MHz
PM4	Off	SPP Link	12 MHz
PM5	On	SPP Link	12 MHz

1. 12MHz used if 32khz not present

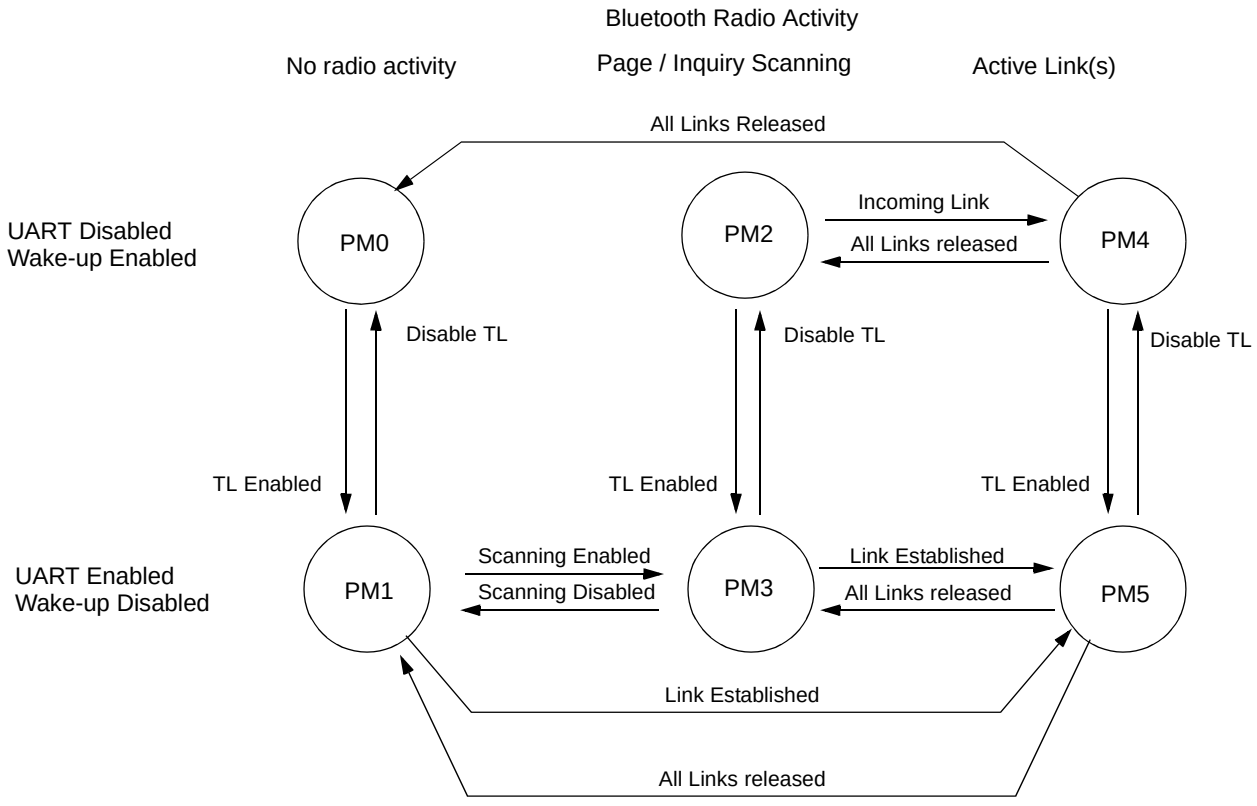


Figure 18. Transition between different Hardware Power Modes

11.0 Power Reduction (Continued)

11.2 UART TRANSPORT LAYER CONTROL

11.2.1 Hardware Wake-Up Functionality

In some circumstances, the host may switch off the transport layer of the LMX9820A to reduce power consumption. The host and LMX9820A then may shut down their UART interfaces.

To simplify the system design, the UART interface is configured for hardware wake-up functionality. For a detailed timing and command functionality, see the “LMX9820A Software Users Guide”.

The interface between the host and LMX9820A is shown in Figure 19.

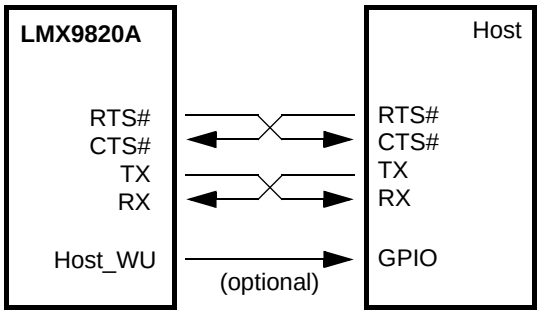


Figure 19. UART Null Modem Connections

11.2.2 Disabling the UART Transport Layer

The host can disable the UART transport layer by sending the “Disable Transport Layer” Command. The LMX9820A will empty its buffers, send the confirmation event, and disable its UART interface. The UART interface will then be reconfigured to wake up the LMX9820A on a falling edge of the CTS pin.

11.2.3 LMX9820A Enabling the UART Interface

Because the transport layer can be disabled in any situation, the LMX9820A must verify that the transport layer is enabled before sending data to the host. Possible situations in which the LMX9820A will need to re-enable the interface include incoming data or incoming link indicators. If the UART is not enabled, the LMX9820A must assume that the host is in a low-power mode and initiate a wake-up event by asserting RTS and setting HOST_WU to 1. To be able to respond to the wake-up event, the host must monitor its CTS input (i.e. the LMX9820A RTS output).

As soon as the host activates its RTS output (i.e. the LMX9820A CTS input), the LMX9820A will first send a confirmation event and then start to transmit the events.

11.2.4 Enabling the UART Transport Layer from Host

If the host needs to send data or commands to the LMX9820A while the UART transport layer is disabled, it must first assume that the LMX9820A is sleeping and wake it up by asserting the host RTS output (i.e. the LMX9820A CTS input).

When the LMX9820A detects the wake-up signal, it enables the UART and acknowledges the wake-up signal by asserting its RTS output and HOST_WU signal. Additionally, the wake-up event will be acknowledged by sending a confirmation event. When the host has received this “Transport Layer Enabled” event, it knows the LMX9820A is ready to receive commands.

12.0 Command Interface

The LMX9820A offers Bluetooth functionality through either a self-contained slave functionality or a simple command interface. The interface is carried over the UART interface.

The following sections describe the protocol on the UART interface between the LMX9820A and the host in command mode (see Figure 20). In Transparent mode, no data framing is necessary and the device does not interpret data carried over the interface as commands.

12.1 FRAMING

The connection is considered “Error free”. But for packet recognition and synchronization, some framing is used.

All packets sent in both directions are constructed following the model shown in Table 27.

12.1.1 Start and End Delimiters

The “STX” character is used as the start delimiter: STX = 0x02. ETX = 0x03 is used as the end delimiter.

12.1.2 Packet Type ID

This byte identifies the type of packet. See Table 28 for details.

12.1.3 Opcode

The opcode identifies the command to execute. The opcode values can be found within the “LMX9820A Software User’s Guide” included with the LMX9820A Evaluation Board.

12.1.4 Data Length

Number of bytes in the Packet Data field. The maximum size is 333 data bytes per packet.

12.1.5 Checksum

This is a simple Block Check Character (BCC) checksum of the bytes “Packet type”, “Opcode”, and “Data Length”. The BCC checksum is calculated as low byte of the sum of all bytes (e.g., if the sum of all bytes is 0x3724, the checksum is 0x24).

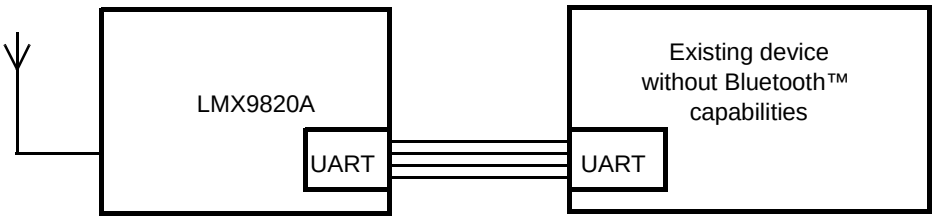


Figure 20. Bluetooth Functionality

.

Table 27. Packet Framing

Start Delimiter	Packet Type ID	Opcode	Data Length	Checksum	Packet Data	End Delimiter
1 Byte	1 Byte	1 Byte	2 Bytes	1 Byte	<Data Length> Bytes	1 Byte
	- - - - - - - - - - - - - Checksum - - - - - - - - - - - - -					

Table 28. Packet Type Identification

ID	Direction	Description
0x52 ‘R’	REQUEST (REQ)	A request sent to the Bluetooth module. All requests are answered by exactly one confirm.
0x43 ‘C’	Confirm (CFM)	The Bluetooth modules confirm to a request. All requests are answered by exactly one confirm.
0x69 ‘i’	Indication (IND)	Information sent from the Bluetooth module that is not a direct confirm to a request. Indicating status changes, incoming links, or unrequested events.
0x72 ‘r’	Response (RES)	An optional response to an indication. This is used to respond to some type of indication message.

12.0 Command Interface (Continued)

12.2 COMMAND SET OVERVIEW

The LMX9820A has a well-defined command set to:

- Configure the device:
  - Hardware settings
  - Local Bluetooth parameters
  - Service database
- Set up and handle links

Tables 29 through 39 show the actual command set and the events coming back from the device. A fully documented description of the commands can be found in the "LMX9820A Software Users Guide".

Note: Additional command details are contained in the Software Users Guide.

Table 29. Device Discovery Commands

Command	Event	Description
Inquiry	Inquiry Complete	Search for devices
	Device Found	Lists BDADDR and class of device
Remote Device Name	Remote Device Name Confirm	Get name of remote device

Table 30. SDAP Client Commands

Command	Event	Description
SDAP Connect	SDAP Connect Confirm	Create an SDP connection to remote device
SDAP Disconnect	SDAP Disconnect Confirm	Disconnect an active SDAP link
	Connection Lost	Notification for lost SDAP link
SDAP Service Browse	Service Browse Confirm	Get the services of the remote device
SDAP Service Search	SDAP Service Search Confirm	Search a specific service on a remote device
SDAP Attribute Request	SDAP Attribute Request Confirm	Searches for services with specific attributes

Table 31. SPP Link Commands

Command	Event	Description
Establish SPP Link	Establishing SPP Link Confirm	Initiates link establishment to a remote device
	Link Established	Link successfully established
	Incoming Link	A remote device established a link to the local device
Set Link Timeout	Set Link Timeout Confirm	Confirms the supervision timeout for the existing link
Get Link Timeout	Get Link Timeout Confirm	Get the supervision timeout for the existing link
Release SPP Link	Release SPP Link Confirm	Initiate release of SPP link
SPP Send Data	SPP Send Data Confirm	Send data to specific SPP port
	Incoming Data	Incoming data from remote device
Transparent Mode	Transparent Mode Confirm	Switch to transparent mode on the UART

Table 32. Default Connection Commands

Command	Event	Description
Connect Default Connection	Connect Default Connection Confirm	Connects to either one or all stored default connections
Store Default Connection	Store Default Connection Confirm	Store device as default connection
Get List of Default Connections	List of Default Devices	
Delete Default Connections	Delete Default Connections Confirm	

12.0 Command Interface (Continued)

Table 33. Power Mode Commands

Command	Event	Description
Set Default Link Policy	Set Default Link Policy Confirm	Defines the link policy used for any incoming or outgoing link.
Get Default Link Policy	Get Default Link Policy Confirm	Returns the stored default link policy
Set Link Policy	Set Link Policy Confirm	Defines the modes allowed for a specific link
Get Link Policy	Get Link Policy Confirm	Returns the actual link policy for the link
Enter Sniff Mode	Enter Sniff Mode Confirm	
Exit Sniff Mode	Exit Sniff Mode Confirm	
Enter Park Mode	Enter Park Mode Confirm	
Enter Hold Mode	Enter Hold Mode Confirm	
	Power Save Mode Changed	Remote device changed the power save mode on the link

Table 34. Audio Control Commands

Command	Event	Description
Establish SCO Link	Establish SCO Link Confirm	Establish SCO link on existing RFComm link
Release SCO Link	Release SCO Link Confirm	Release SCO link
	SCO Link Established Indicator	A remote device has established a SCO link to the local device
	SCO Link Released Indicator	SCO link has been released
Change SCO Packet Type	Change SCO Packet Type Confirm	Changes packet type for existing SCO link
	SCO Packet Type changed indicator	SCO packet type has been changed
Set Audio Settings	Set Audio Settings Confirm	Set audio settings for existing link
Get Audio Settings	Get Audio Settings Confirm	Get audio settings for existing link
Set Volume	Set Volume Confirm	Configure the volume
Get Volume	Get Volume Confirm	Get current volume setting
Mute	Mute Confirm	Mutes the microphone input

Table 35. Wake Up Function Commands

Command	Event	Description
Disable Transport Layer	Transport Layer Enabled	Disabling the UART transport layer and activates the hardware wake-up function

12.0 Command Interface (Continued)

Table 36. SPP Port Configuration and Status Commands

Command	Event	Description
Set Port Config	Set Port Config Confirm	Set port setting for the “virtual” serial port link over the air
Get Port Config	Get Port Config Confirm	Read the actual port settings for a “virtual” serial port
	Port Config Changed	Notification if port settings were changed from remote device
SPP Get Port Status	SPP Get Port Status Confirm	Returns status of DTR and RTS (for the active RFComm link)
SPP Port Set DTR	SPP Port Set DTR Confirm	Sets the DTR bit on the specified link
SPP Port Set RTS	SPP Port Set RTS Confirm	Sets the RTS bit on the specified link
SPP Port BREAK	SPP Port BREAK	Indicates that the host has detected a break
SPP Port Overrun Error	SPP Port Overrun Error Confirm	Used to indicate that the host has detected an overrun error
SPP Port Parity Error	SPP Port Parity Error Confirm	Host has detected a parity error
SPP Port Framing Error	SPP Port Framing Error Confirm	Host has detected a framing error
	SPP Port Status Changed	Indicates that remote device has changed one of the port status bits

Table 37. Local Settings Commands

Command	Event	Description
Read Local Name	Read Local Name Confirm	Read user-friendly name of the device
Write Local Name	Write Local Name Confirm	Set the user-friendly name of the device
Read Local BDADDR	Read Local BDADDR Confirm	
Change Local BDADDR	Change Local BDADDR Confirm	**Note:** Only use if you have your own BDADDR pool
Store Class of Device	Store Class of Device Confirm	
Set Scan Mode	Set Scan Mode Confirm	Change mode for discoverability and connectability
	Set Scan Mode Indication	Reports end of automatic limited discoverable mode
Get Fixed Pin	Get Fixed Pin Confirm	Reads current PinCode stored within the device
Set Fixed Pin	Set Fixed Pin Confirm	Set the local PinCode
Get Security Mode	Get Security Mode Confirm	Get actual Security mode
Set Security Mode	Set Security Mode Confirm	Configure Security mode for local device (default 2)
Remove Pairing	Remove Pairing Confirm	Remove pairing with a remote device
List Paired Devices	List of Paired Devices	Get list of paired devices stored in the LMX9820A data memory
Set Default Link Timeout	Set Default Link Timeout Confirm	Store default link supervision timeout
Get Default Link Timeout	Get Default Link Timeout Confirm	Get stored default link supervision timeout
Force Master Role	Force Master Role Confirm	Enables/Disables the request for master role at incoming connections

12.0 Command Interface (Continued)

Table 38. Local Service Database Configuration Commands

Command	Event	Description
Store SPP Record	Store SPP Record Confirm	Create a new SPP record within the service database
Store DUN Record	Store DUN Record Confirm	Create a new DUN record within the service database
Store FAX Record	Store FAX Record Confirm	Create a new FAX record within the service database
Store OPP Record	Store OPP Record Confirm	Create a new OPP record within the service database
Store FTP Record	Store FTP Record Confirm	Create a new FTP record within the service database
Store IrMCSync Record	Store IrMCSync Record Confirm	Create a new IrMCSync record within the service database
Enable SDP Record	Enable SDP Record Confirm	Enable or disable SDP records
Delete All SDP Records	Delete All SDP Records Confirm	
Ports to Open	Ports to Open Confirmed	Specify the RFComm Ports to open on startup

Table 39. Local Hardware Commands

Command	Event	Description
Set Default Audio Settings	Set Default Audio Settings Confirm	Configure default settings for audio codec and air format, stored in NVS
Get Default Audio Settings	Get Default Audio Settings Confirm	Get stored default audio settings
Set Event Filter	Set Event Filter Confirm	Configures the reporting level of the command interface
Get Event Filter	Get Event Filter Confirm	Get the status of the reporting level
Read RSSI	Read RSSI Confirm	Returns an indicator for the incoming signal strength
Change UART Speed	Change UART Speed Confirm	Set specific UART speed; needs proper ISEL pin setting
Change UART Settings	Change UART Settings Confirm	Change configuration for parity and stop bits
Test Mode	Test Mode Confirm	Enable Bluetooth, EMI test, or local loopback
Restore Factory Settings	Restore Factory Settings Confirm	
Reset	Dongle Ready	Soft reset
Firmware Upgrade		Stops the Bluetooth firmware and executes the in-system programming code

13.0 Usage Scenarios

13.1 SCENARIO 1: POINT-TO-POINT CONNECTION

LMX9820A acts only as slave, no further configuration is required.

Example: Sensor with LMX9820A; hand-held device with standard Bluetooth option.

The SPP conformance of the LMX9820A allows any device using the SPP to connect to the LMX9820A.

By switching to transparent mode automatically, the controller has no need for an additional protocol layer; data is sent raw to the other Bluetooth device.

On default, a PinCode is requested to block unallowed targeting.

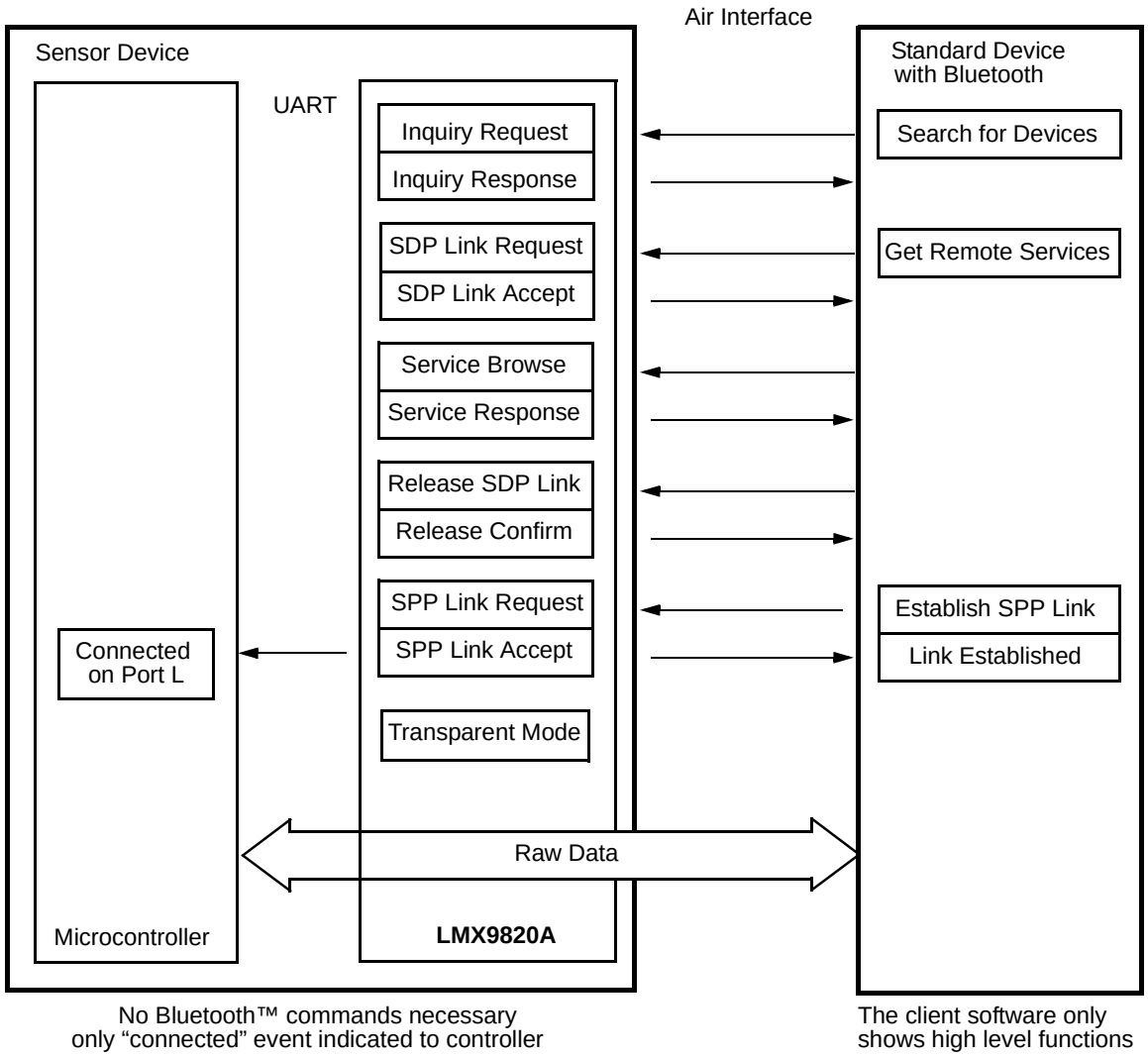


Figure 21. Point-to-Point Connection

13.0 Usage Scenarios (Continued)

13.2 SCENARIO 2: AUTOMATIC POINT-TO-POINT CONNECTION

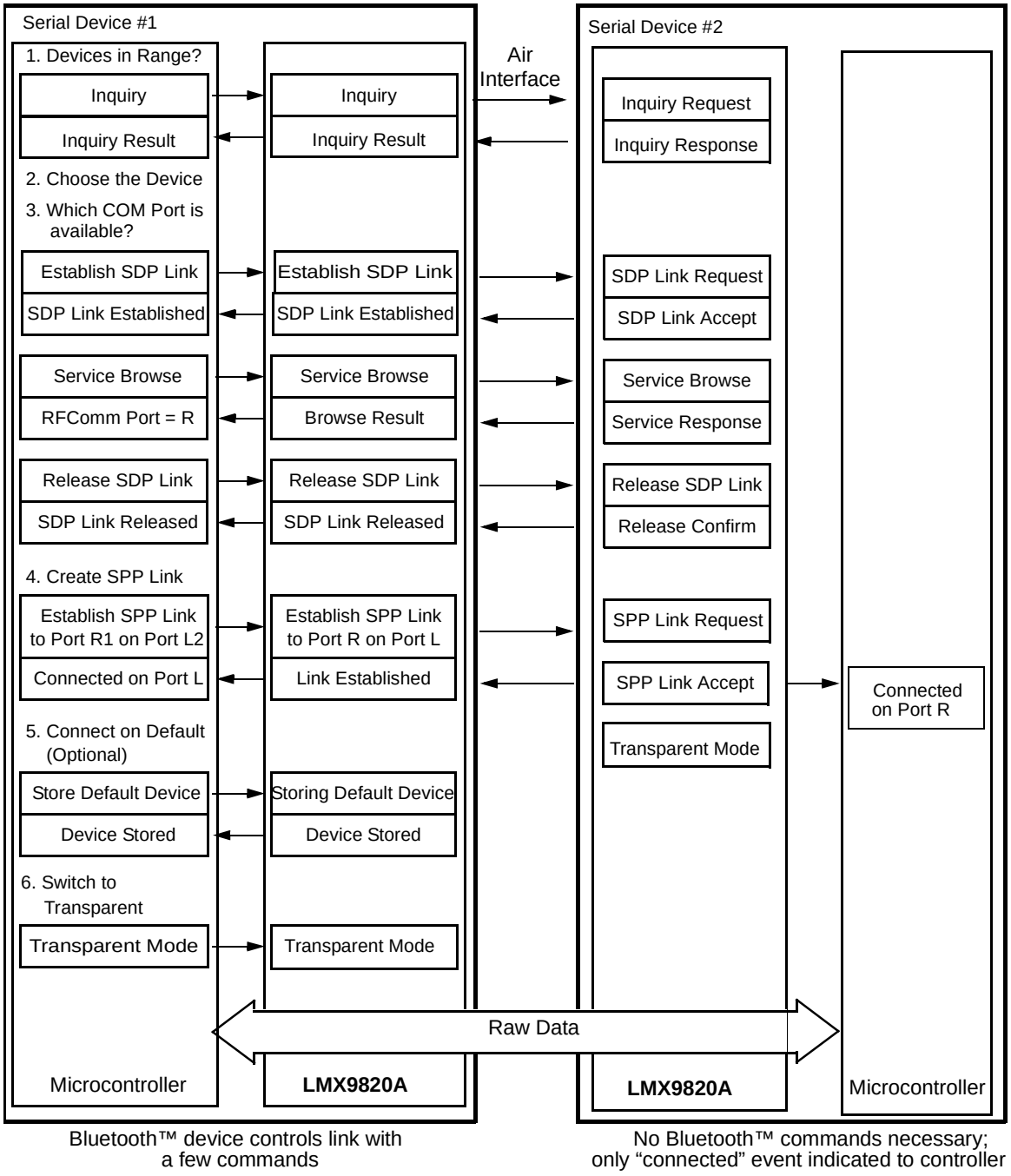
LMX9820A at both sides.

Example: Serial Cable Replacement.

Device #1 controls the link setup with a few commands as described.

If step 5 is executed, the stored default device is connected (step 4) after reset (in automatic mode only) or by sending the “Connect to Default Device” command. The command can be sent to the device at any time.

If step 6 is left out, the microcontroller has to use the “Send Data” command, instead of sending data directly to the module.



1. Port R indicates the remote RFComm channel to connect to. Usually the result of the SDP request.
2. Port L indicates the Local RFComm channel used for that connection.

Figure 22. Automatic Point-to-Point Connection

13.0 Usage Scenarios (Continued)

13.3 SCENARIO 3: POINT-TO-MULTIPOINT CONNECTION

LMX9820A acts as master for several slaves.

Example: Two sensors with LMX9820A; one hand-held master device with LMX9820A.

Serial Devices #2 and #3 establish the link automatically as soon as they are contacted by another device. No controller interaction is necessary for setting up the Bluetooth link. Both switch automatically into transparent mode. The host sends raw data over the UART.

Serial Device #1 is acting as master for both devices. The host controls which device is sending data, using the “Send data” command. If the device receives data from the other devices, it is packaged into an “Incoming data” event. The event includes the device related port number.

If necessary, a link configuration can be stored as default in the master Serial Device #1 to enable the automatic reconnect after reset, power-up, or by sending the “connect default connection” command.

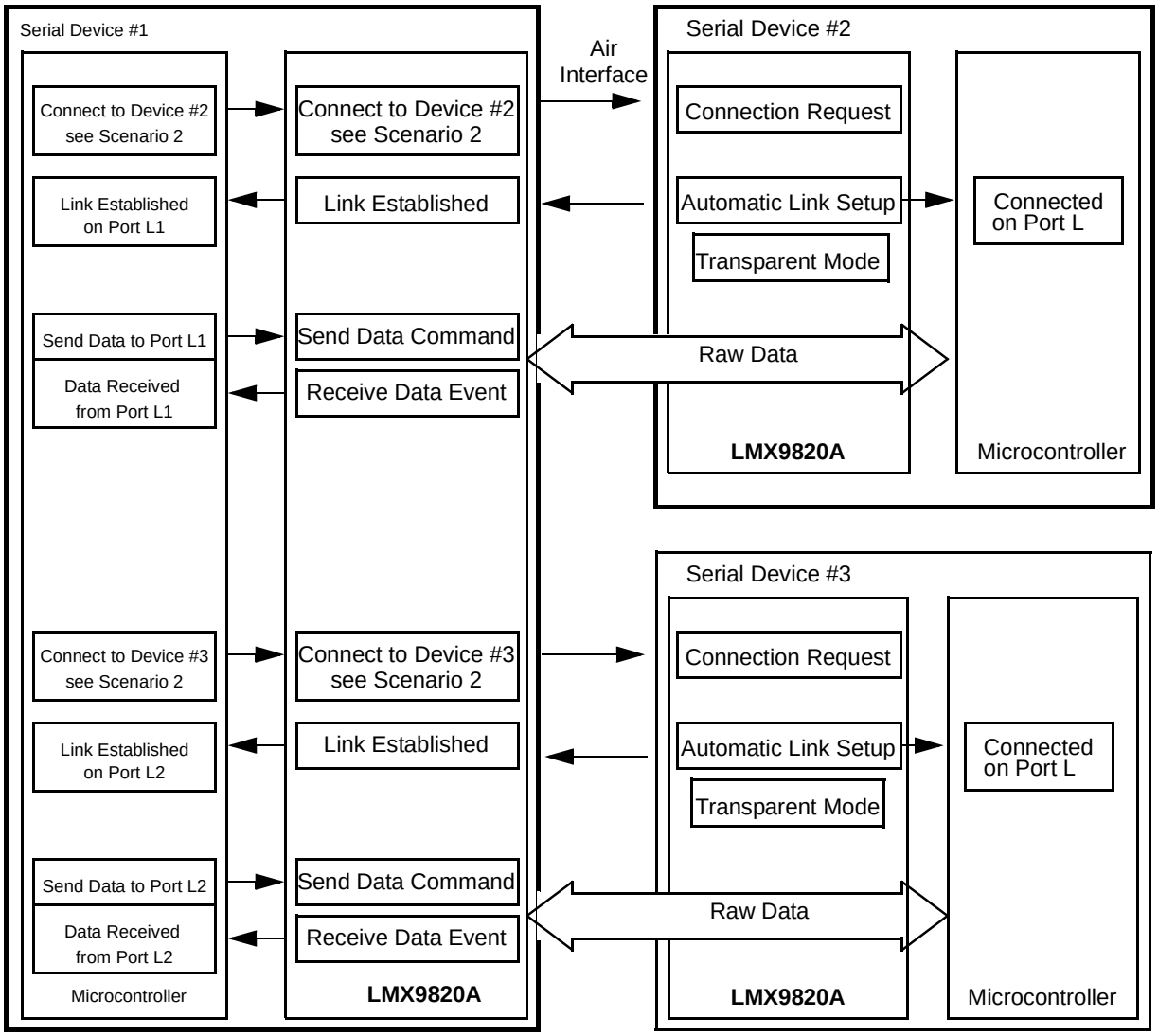


Figure 23. Point-to-Multipoint Connection

14.0 Application Information

Figure 24 on page 35 represents a typical system schematic with optional 32KHz mounted for the LMX9820A.

14.1 MATCHING NETWORK

The antenna matching network may or may not be required, depending upon the impedance of the antenna chosen. A 6.8 pF blocking capacitor is recommended.

14.2 FILTERED POWER SUPPLY

It is important to provide the LMX9820A with adequate ground planes and a filtered power supply. It is highly recommended that a 0.1 µF and a 10 pF bypass capacitor be placed as close as possible to V_{CC} (pad H2) on the LMX9820A.

14.3 HOST INTERFACE

To set the logic thresholds of the LMX9820A to match the host system, IOV_{CC} (pad H12) must be connected to the logic power supply of the host system. It is highly recommended that a 10 pF bypass capacitor be placed as close as possible to the IOV_{CC} pad on the LMX9820A.

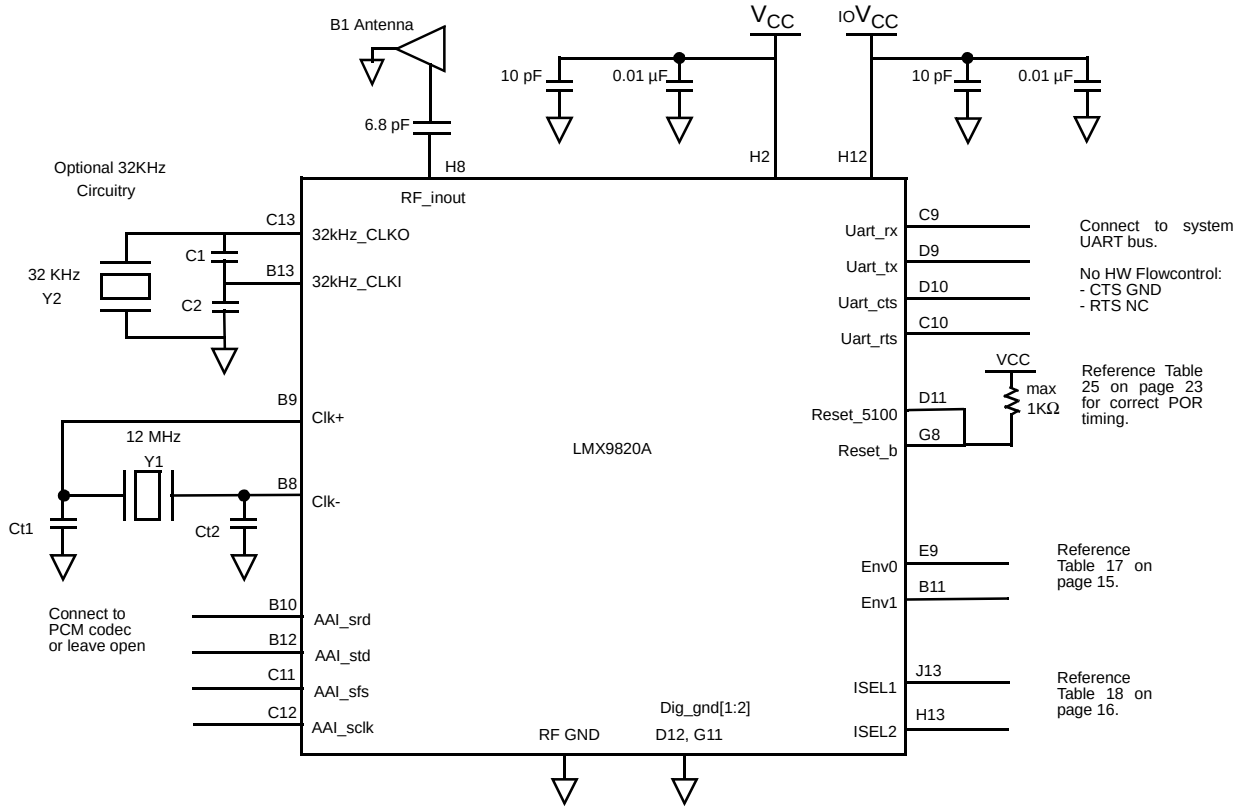
ISEL2 (pad H13) and ISEL1 (pad J13) can be strapped to the host logic 0 and 1 levels to set the host interface boot-up configuration. Alternatively both ISEL2 and ISEL1 can be hardwired over 10kΩ pullup/pulldown resistors.

Env0 (pad E9) and Env1 (pad B11) can be left unconnected (both are pulled high), if no ISP capability is required. If the ISP environment mode is needed, then Env0 must be driven to logic low and Reset needs to be asserted. After de-assertion of Reset, the LMX9820A boots into the mode corresponding to the values present on Env0 and Env1. Alternatively, a firmware upgrade command can be used.

14.4 CLOCK INPUT

The clock source must be placed as close as possible to the LMX9820A. The quality of the radio performance is directly related to the quality of the clock source connected to the oscillator port on the LMX9820A. Careful attention must be paid to the crystal/oscillator parameters or radio performance could be drastically reduced.

14.5 SCHEMATIC AND LAYOUT EXAMPLES



Notes:

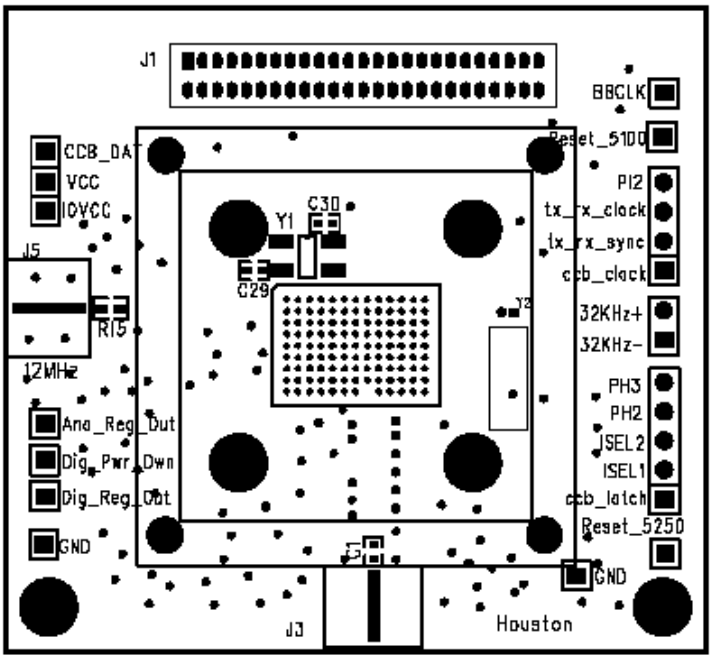
Capacitor values, Ct1, Ct2, C1 and C2 may vary depending on board design crystal manufacturer specification.

Single ground plane is used for both RF and digital grounds.

Recommend that a 4 component T-PI pad be used between RF output and antenna. This allows for versatility in the design such that the match to the antenna maybe improved and/or the blocking margin increased by use a LC filter.

Figure 24. Example System Schematic

14.0 Application Information (Continued)



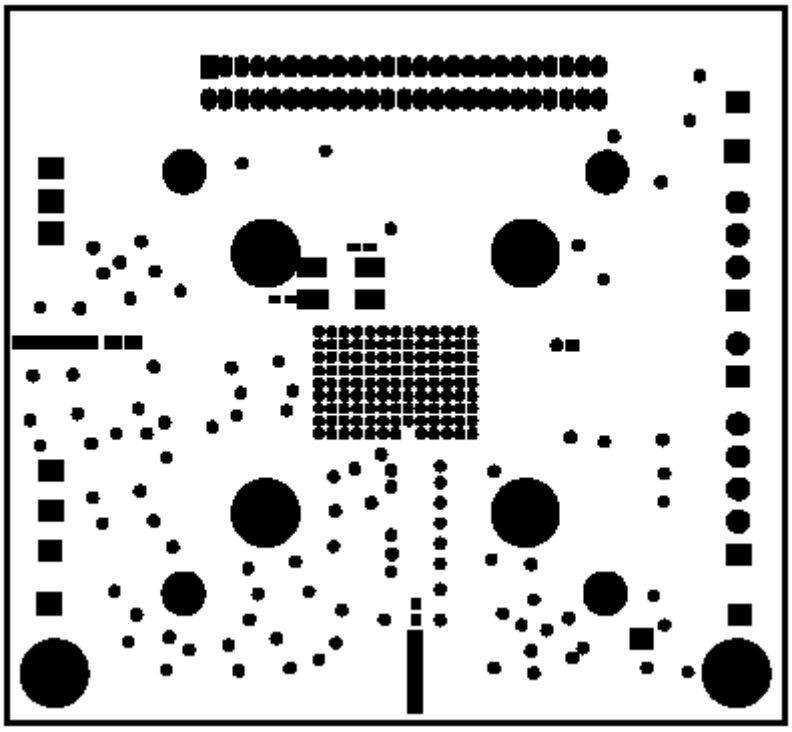


Figure 25. Component Placement (Layer 1)

14.0 Application Information (Continued)

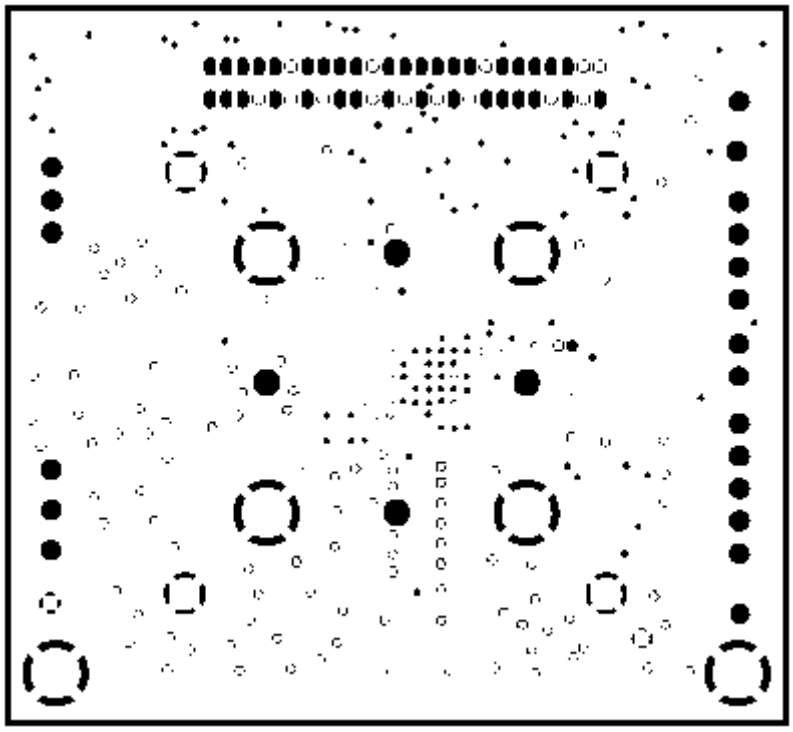


Figure 26. Solid Ground Plane (Layer 2)

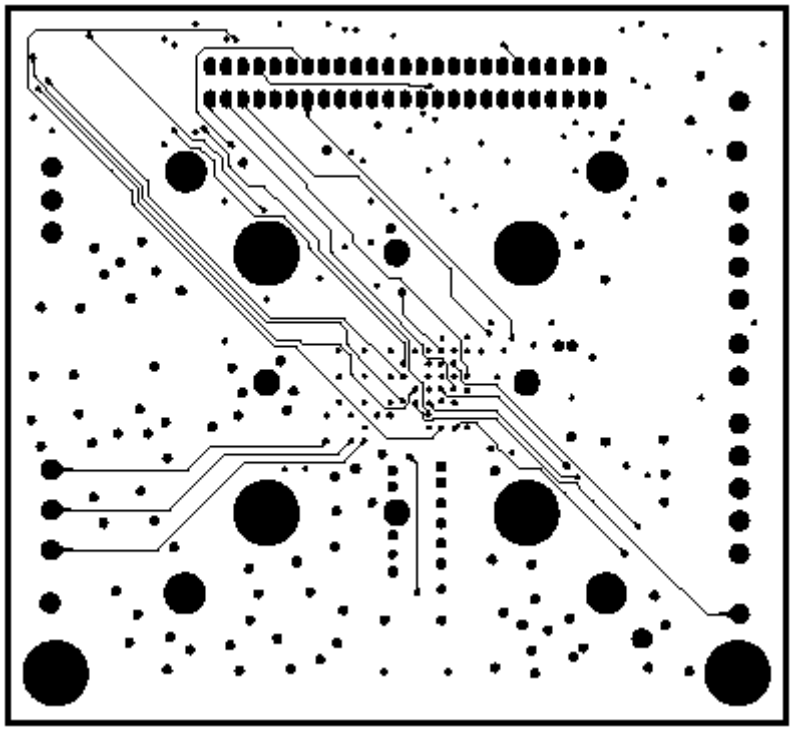


Figure 27. Signal Plane (Layer 3)

14.0 Application Information (Continued)

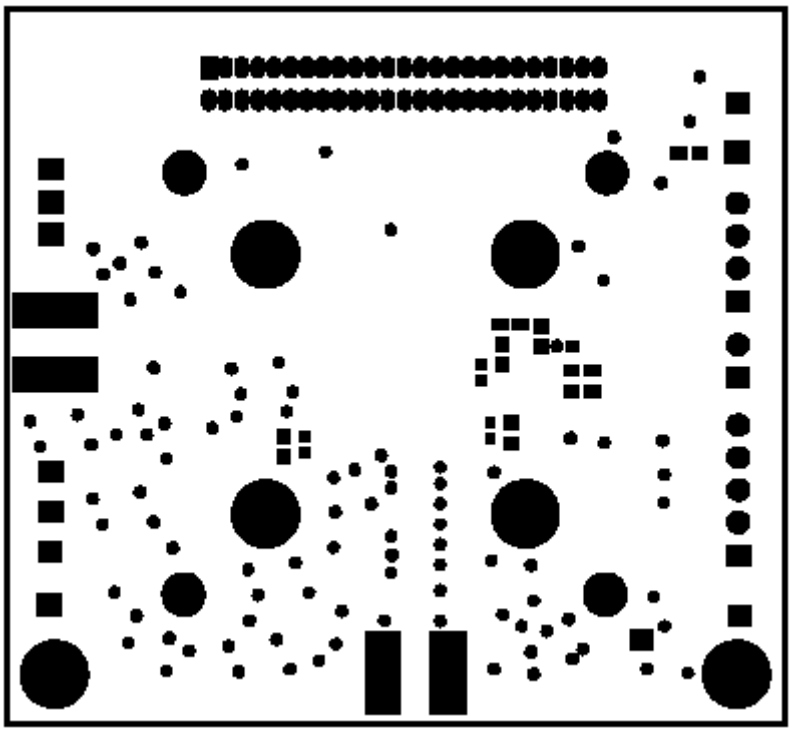
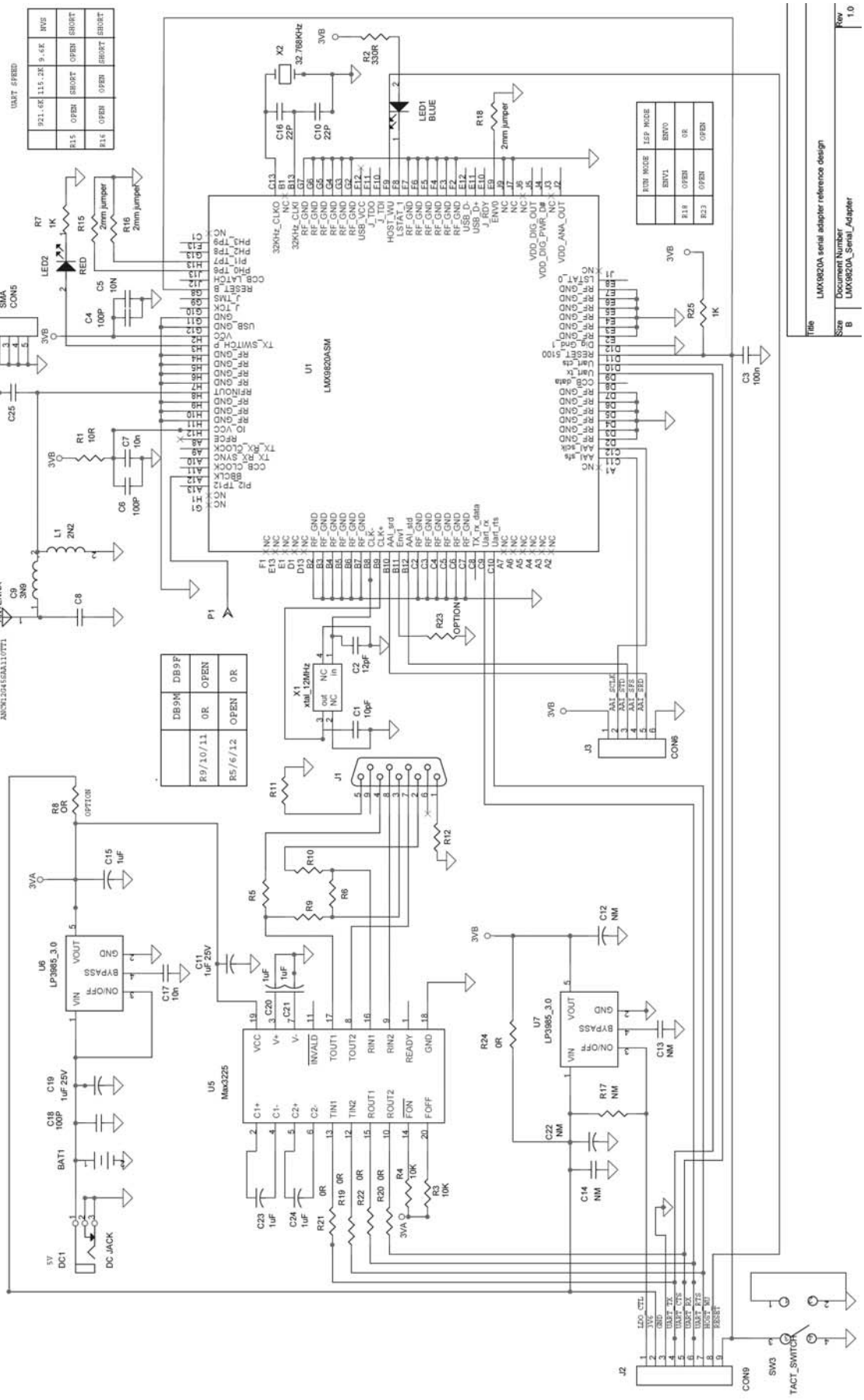


Figure 28. Component Layout Bottom (Layer 4)

15.0 Reference Design



16.0 Soldering

The LMX9820A bumps are designed to melt as part of the Surface Mount Assembly (SMA) process. In order to ensure reflow of all solder bumps and maximum solder joint reliability while minimizing damage to the package, recommended reflow profiles should be used.

Table 40, Table 41 and Figure 29 on page 41 provide the soldering details required to properly solder the LMX9820A to standard PCBs. The illustration serves only as a guide and National is not liable if a selected profile does not work.

See IPC/JEDEC J-STD-020C, July 2004 for more information

Table 40. Soldering Details

Parameter	Value
PCB Land Pad Diameter	24 mil
PCB Solder Mask Opening	30 mil
PCB Finish (HASL details)	Defined by customer or manufacturing facility
Stencil Aperture	28 mil
Stencil Thickness	5 mil
Solder Paste Used	Defined by customer or manufacturing facility
Flux Cleaning Process	Defined by customer or manufacturing facility
Reflow Profiles	See Figure 29 on page 41

Table 41. Classification Reflow Profiles[1, 2]

Profile Feature	Sn-Pb Eutectic Assembly	NOPB Assembly
Average Ramp-Up Rate (Ts_{MAX} to Tp)	3°C/second maximum	3°C/second maximum
Preheat: Temperature Min (Ts_{MIN}) Temperature Max (Ts_{MAX}) Time (ts_{MIN} to ts_{MAX})	 100°C 150°C 60–120 seconds	 150°C 200°C 60–180 seconds
Time maintained above: Temperature (T_L) Time (t_L)	 183°C 60–150 seconds	 217°C 60–150 seconds
Peak/Classification Temperature (Tp)	225 +0/-5°C	260 + 0°C
Time within 5°C of actual Peak Temperature (tp)	10–30 seconds	20–40 seconds
Ramp-Down Rate	6°C/second maximum	6°C/second maximum
Time 25 °C to Peak Temperature	6 minutes maximum	8 minutes maximum
Reflow Profiles	See Figure 29	See Figure 29

1. See IPC/JEDEC J-STD-020C, July 2004.
2. All temperatures refer to the top side of the package, measured on the package body surface.

16.0 Soldering (Continued)

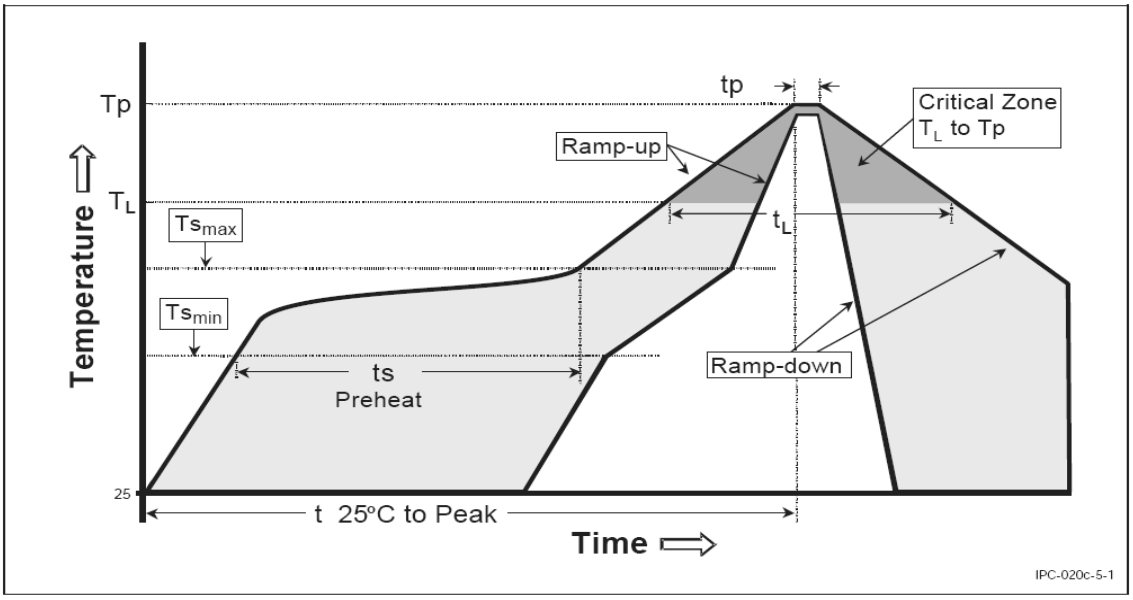


Figure 29. Typical Reflow Profiles

17.0 Datasheet Revision History

This section is a report of the revision/creation process of the datasheet for the LMX9820A. Table 42 provides the stages/definitions of the datasheet. Table 43 lists the revision history.

Table 42. Documentation Status Definitions

Datasheet Status	Product Status	Definition
Advance Information	Formative or in Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data. Supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.S
No Identification Noted	Full production	This datasheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not in Production	This datasheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The datasheet is printed for reference information only.

Table 43. Revision History

Revision # (PDF Date)	Revisions/Comments
0.4 (April 2003)	Initial Datasheet revised to include new radio and additional functionality. Several edits have been made to functional, performance, and electrical details.
0.6 (February 2004)	Updated RF performance values Added 32 kHz frequency support.
0.7 (August 2004)	Updated General Description and Features with Audio Updated Pinout Information Added Audio Section Updated Command Section with audio commands
0.71 (August 2004)	Reviewed Crystal Support Section Added Audio block to application diagram
0.72 (October 2004)	Updated package size Table 9 to Table 15 updated Optional 32.768 kHz crystal support removed Package outline drawing updated to 14.1mm width and 2.0mm height
0.73 (December 2004)	In Table 15, maximum output power range updated to +4dBm.
0.80 (March 2005)	Minor edits for clarity, language, units, formatting, etc. No functional changes.
0.81 (March 2005)	Minor changes in feature list Table 2 updated Added footnote to Table 10 Added description in chapter 6.2 Table 20 updated
0.82 (March 2005)	Added footnote to Table 13 Figure 22 updated
1.0 draft 1 (March 2005)	Updated Power consumption Table 12

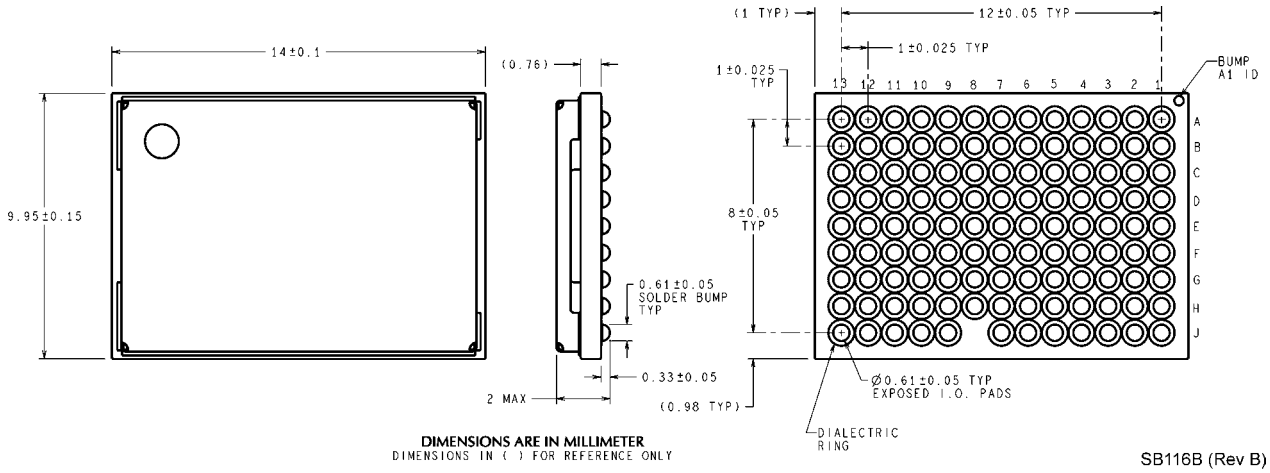
17.0 Datasheet Revision History (Continued)

Table 43. Revision History

Revision # (PDF Date)	Revisions/Comments
1.0 draft 2 (April 2005)	No functional Update
1.0 draft 3 (April 2005)	Updated C/I in Table 14
1.0 (April 2005)	No functional Update
1.1	Interim internal release.
1.2 (May 2006)	NOPB added, 32.768kHz oscillator, WinBond and PCM slave info, sniff mode, Reference to NKG3184A TCXO removed.
1.3 (September 2006)	In the pad descriptions table, H4 changed to RF GND not NC. Reference Schematic section added, Low power section completed, System schematic completed with 32KHz crystal option.

Note

18.0 Physical Dimension



NOTES:

PAD PITCH IS 1.00 MILLIMETER (.0394") NON-ACCUMULATIVE.

UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN MILLIMETER.

TOLERANCE, UNLESS OTHERWISE SPECIFIED:
TWO PLACE (.00): ±.01
THREE PLACE (.000): ±.002
ANGULAR: ±1°

Figure 30. Package with Sn-Pb Solder Bumps (metal housing).

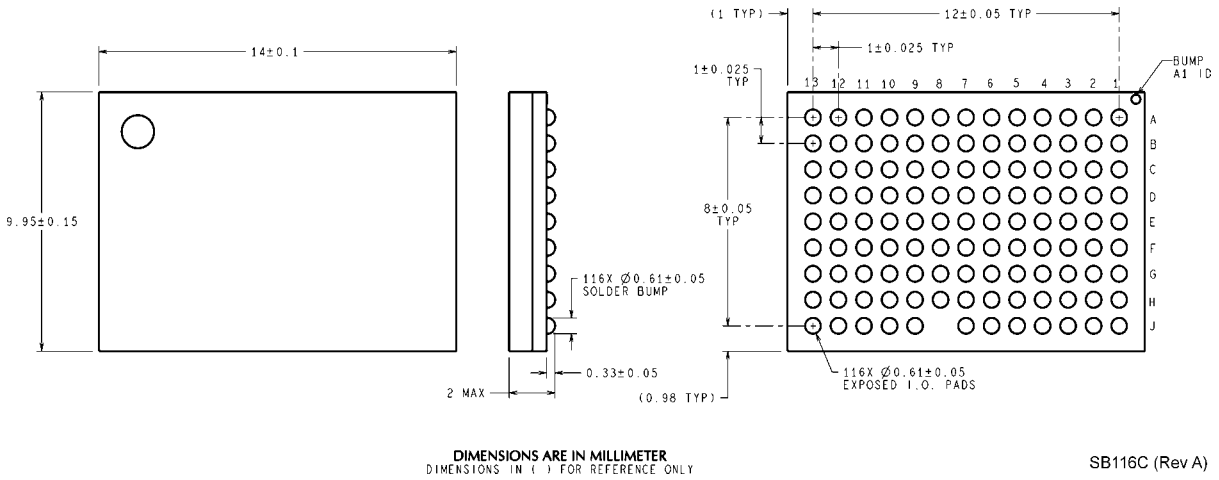


Figure 31. Package with NOPB Solder Bumps (plastic housing).

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